VOLTAGE REGULATORS
OP AMPS & COMPARATORS
1st EDITION
ISSUED AUGUST 1983

INTRODUCTION

This book contains datasheets for SGS monolithic voltage regulators, operational amplifiers and comparators. Also included are a selection of darlington arrays.
Other SGS bipolar ICs are listed on pages 341 to 356. Datasheets for these products are included in the databooks:

- POWER LINEAR ACTUATORS
- AUDIO, RADIO AND TV CIRCUITS
- TELECOM PRODUCTS

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ALPHANUMERICAL INDEX

SELECTOR GUIDE

Voltage Regulators

STANDARD – Positive

I_o max (A)	Type	Regulated output voltage (V)											Package
		5	6	7.5	8	9	10	12	15	18	20	24	
2 (*)	L78S00CV	●		●		●	●	●	●	●		●	TO-220
	L78S00CT/T	●		●		●	●	●	●	●		●	TO-3
1.5	LM117K	1.2V ← adjustable → 37V											TO-3
	LM217K												TO-3
	LM317K												TO-3
	LM317T												TO-220
1	L7800CV	●	●		●			●	●	●	●	●	TO-220
	L7800ACV(**)	●	●		●			●	●	●	●	●	TO-220
	L7800CT/T	●	●		●			●	●	●	●	●	TO-3
0.5	L78M00CV	●	●		●			●	●	●	●	●	TO-220
	L78M00CX	●	●		●			●	●	●	●	●	SOT-82
	L123CB	2V ← adjustable → 36V											DIP-14
	L123CTB												TO-100
	L123TB												TO-100
	LM723CB												TO-100
	LM723CTB												TO-100
0.15	LM723TB												TO-100
	L146CB	2V ← adjustable → 77V											DIP-14
	L146CTB												TO-100
	L146TB												TO-100

STANDARD – Negative

I_o max (A)	Type	Regulated output voltage (V)								Package
		-5	-5.2	-8	-12	-15	-18	-20	-24	
1	L7900ACV(**)	●	●	●	●	●	●	●	●	TO-220
	L7900CV	●	●	●	●	●	●	●	●	TO-220
	L7900CT/T	●	●	●	●	●	●	●	●	TO-3

(*) Proprietary SGS selection.
(**) Output voltage = ± 2%.

Voltage Regulators

LOW DROP

Type	Low drop	Very low drop	Transient protection ±100	Transient protection ± 80	Transient protection ± 60	Transient protection ± 40	Reset	Short circuit protection	Reverse voltage protection	Output voltage 5V	Output voltage 8.5V	Output voltage 10V
L387		●					●	●	●	●		
L487		●		●			●	●	●	●		
L2605	●		●					●	●	●		
L2685	●		●					●	●		●	
L2610	●		●					●	●			●
L4705		●		●				●	●	●		
L4785		●		●				●	●		●	
L4710		●		●				●	●			●
L4805		●			●			●	●	●		
L4885		●			●			●	●		●	
L4810		●			●			●	●			●
LM2930A		●				●		●	●	●		
LM2931A		●			●			●	●	●		

PROPRIETARY

I_o max (A)	Type	Regulated output voltage (V)	5	8.5	10		Package
4	L296 (*)	5.1V ← adjustable → 40V					Multiwatt 15
2	L200CH/CV L200CT/T	2.9V ← adjustable → 36V					Pentawatt TO-3(4 lead)
0.5	L387		●				Pentawatt
	L487		●				Pentawatt
	L2600V		●	●	●		TO-220
	L4700CV		●	●	●		TO-220
	L4800CV		●	●	●		TO-220
0.4	LM2930A		●				TO-220
	LM2931A		●				TO-220

(*) Switch mode power supply.

Operational Amplifiers

SINGLE

Type	Temperature Range (°C)	Frequency compensat.	CMR (dB)	Input Bias Curr. (nA)	Slew Rate (V/µs)	Max supply Voltage (V)	Package
LM741TB	-55 to 125	●	90	80	0.5	± 22	TO-99
LM741ATB	-55 to 125	●	95	30	0.7	± 22	
LM741CTB	0 to 70	●	90	80	0.5	± 18	
LM748TB	-55 to 125		90	80	5.5	± 22	
LM748ATB	-55 to 125		95	20	5.5	± 22	
LM748CTB	0 to 70		90	80	5.5	± 22	
LS101TB	-55 to 125		90	120	10	± 22	
LS101ATB	-55 ro 125		96	30	10	± 22	
LS107TB	-55 to 125	●	96	30	0.7	± 22	
LS141TB	-55 to 125	●	90	80	0.5	± 22	
LS141ATB	-55 to 125	●	95	30	0.7	± 22	
LS141CTB	0 to 70	●	90	80	0.5	± 18	
LS148TB	-55 to 125		90	80	5.5	± 22	
LS148ATB	-55 to 125		95	20	5.5	± 22	
LS148CTB	0 to 70		90	80	5.5	± 22	
LS201TB	0 to 70		90	250	10	± 22	
LS201ATB	-25 to 85		96	30	10	± 22	
LS207TB	-25 to 85	●	96	30	0.7	± 22	
LS301ATB	0 to 70		90	70	10	± 18	
LS307TB	0 to 70	●	90	70	0.5	± 18	
LS709TB	-55 to 125		90	200	0.25	± 18	
LS709ATB	-55 to 125		110	100	0.25	± 18	
LS709CTB	0 to 70		90	300	0.25	± 18	
LS776TB	-55 to 125	●	90	15	0.35	± 18	
LS776CTB	0 to 70	●	90	15	0.8	± 18	
LM741CB	0 to 70	●	90	80	0.5	± 18	Minidip
LM748CB	0 to 70		90	80	5.5	± 22	
LS141CM	0 to 70	●	90	80	0.5	± 18	
LS148CB	0 to 70		90	80	5.5	± 22	
LS201B	0 to 70		90	250	10	± 22	
LS301AB	0 to 70		90	70	10	± 18	
LS307B	0 to 70	●	90	70	0.5	± 18	
LS776CB	0 to 70	●	90	15	0.8	± 18	
LS141CM	0 to 70	●	90	80	0.5	± 18	SO-8
LC148CM	0 to 70		90	80	5.5	± 22	
LS201M	0 to 70		90	250	10	± 22	
LS301AM	0 to 70		90	70	10	± 18	
LS307M	0 to 70	●	90	70	0.5	± 18	
LS776CM	0 to 70	●	90	15	0.8	± 18	
LS709CB	0 to 70		90	300	0.25	± 18	DIP-14

DUAL

Type	Temperature Range (°C)	Frequency compensat.	CMR (dB)	Input Bias Curr. (nA)	Slew Rate (V/μs)	Max supply Voltage (V)	Package
LM358N	0 to 70	●	70	45	–	32	Minidip
LM358AN	0 to 70	●	85	45	–	32	
LM2904N	-40 to 85	●	70	45	–	26	
LS204CB	0 to 70	●	95	80	1	± 18	
LS4558NB	0 to 70	●	90	50	1.5	± 18	
MC1458P1	0 to 70	●	90	80	0.5	± 18	
MC1458CP1	0 to 70	●	90	80	0.5	± 18	
TDA2320	0 to 70	●	–	100	1.5	20	
TDA2320A	0 to 70	●	–	150	1.6	36	
LS204TB	-25 to 85	●	100	50	1.5	± 18	TO-99
LS204ATB	-55 to 125	●	100	50	1.5	± 18	
LS204CTB	0 to 70	●	95	80	1	± 18	
LM358CM	0 to 70	●	70	45	–	32	SO-8
LM2904CM	-40 to 85	●	70	45	–	26	
LS204M	-25 to 85	●	100	50	1.5	± 18	
LS204CM	0 to 70	●	95	80	1	± 18	
LS4558NM	0 to 70	●	90	50	1.5	± 18	
MC1458M	0 to 70	●	90	80	0.5	± 18	
MC1458CM	0 to 70	●	90	80	0.5	± 18	

QUAD

Type	Temperature Range (°C)	Frequency compensat.	CMR (dB)	Input Bias Curr. (nA)	Slew Rate (V/μs)	Max supply Voltage (V)	Package
LM324N	0 to 70	●	70	45	–	32	DIP-14
LM324AN	0 to 70	●	85	45	–	32	
LM2902N	-40 to 85	●	70	45	–	26	
LS404CB	0 to 70	●	90	100	1	± 18	
LM324CM	0 to 70	●	70	45	–	32	SO-14
LM2902CM	-40 to 85	●	70	45	–	26	
LS404M	0 to 70	●	94	50	1.5	± 18	
LS404CM	0 to 70	●	90	100	1	± 18	

Comparators

DUAL

Type	Temperature Range (°C)	Offset Voltage (mV)	Input bias Current (nA)	Voltage Gain (dB)	Supply Current (mA)	Max supply Voltage (V)	Package
LM393N	0 to 70	2	25	106	0.4	36	Minidip
LM393AN	0 to 70	1	25	106	0.4	36	
LM2903N	-40 to 85	2	25	106	0.4	36	
LM393CM	0 to 70	2	25	106	0.4	36	SO-8
LM2903CM	-40 to 85	2	25	106	0.4	36	

QUAD

Type	Temperature Range (°C)	Offset Voltage (mV)	Input bias Current (nA)	Voltage Gain (dB)	Supply Current (mA)	Max. supply Voltage (V)	Package
LM339N	0 to 70	2	25	106	0.8	36	DIP-14
LM339AN	0 to 70	1	25	106	0.8	36	
LM2901N	-40 to 85	2	25	106	0.8	36	
NC3302P	-40 to 85	3	30	90	0.8	28	
LM339CM	0 to 70	2	25	106	0.8	36	SO-14
LM2901CM	-40 to 85	2	25	106	0.8	36	

Darlington Arrays

Type	N°	V_{CEX}	I_o	Input	Configuration	Package
L201	7	50V	0.5A	General purpose	● —▶|—	DIP-16
L202	7	50V	0.5A	14-25V PMOS	● —▶|—	DIP-16
L203	7	50V	0.5A	5V TTL/CMOS	● —▶|—	DIP-16
L204	7	50V	0.5A	6-15V CMOS/AMOS	● —▶|—	DIP-16
L601	8	90V	0.5A	General purpose	● —▶|—	DIP-18
L602	8	90V	0.4A	14-25V PMOS	● —▶|—	DIP-18
L603	8	90V	0.4A	5V TTL/CMOS	● —▶|—	DIP-18
L604	8	90V	0.4A	6-15V CMOS/PMOS	● —▶|—	DIP-18
ULN2001A	7	50V	0.5A	General purpose	● —▶|—	DIP-16
ULN2002A	7	50V	0.5A	14-25V PMOS	● —▶|—	DIP-16
ULN2003A	7	50V	0.5A	5V TTL/CMOS	● —▶|—	DIP-16
ULN2004A	7	50V	0.5A	6-15V CMOS/PMOS	● —▶|—	DIP-16
ULN2064B	4	50V	1.5A	5V TTL/CMOS	● —▶|—	DIP-16
ULN2065B	4	80V	1.5A	5V TTL/CMOS	● —▶|—	DIP-16
ULN2066B	4	50V	1.5A	6-15V CMOS/PMOS	● —▶|—	DIP-16
ULN2067B	4	80V	1.5A	6-15V CMOS/PMOS	● —▶|—	DIP-16
ULN2068B	4	50V	1.5A	5V CMOS/TTL	▷ ● —▶|—	DIP-16
ULN2069B	4	80V	1.5A	5V CMOS/TTL	▷ ● —▶|—	DIP-16
ULN2070B	4	50V	1.5A	6-15V CMOS/PMOS	▷ ● —▶|—	DIP-16
ULN2071B	4	80V	1.5A	6-15V CMOS/PMOS	▷ ● —▶|—	DIP-16
ULN2074B	4	50V	1.5A	General purpose	■	DIP-16
ULN2075B	4	80V	1.5A	General prupose	■	DIP-16
ULN2076B	4	50V	1.5A	6-15V CMOS/PMOS	■	DIP-16
ULN2077B	4	80V	1.5A	6-15V CMOS/PMOS	■	DIP-16
ULN2801A	8	50V	0.5A	General purpose	● —▶|—	DIP-18
ULN2802A	8	50V	0.5A	14-25V PMOS	● —▶|—	DIP-18
ULN2803A	8	50V	0.5A	5V TTL/CMOS	● —▶|—	DIP-18
ULN2804A	8	50V	0.5A	6-15V CMOS/PMOS	● —▶|—	DIP-18
ULN2805A	8	50V	0.5A	High Output TTL	● —▶|—	DIP-18

● = common emitters;
—▶|— = integral suppression diodes;
■ = isolated darlingtons;
▷ = predriver stage.

DATASHEETS

SGS

L123
L123C

LINEAR INTEGRATED CIRCUITS

HIGH PRECISION VOLTAGE REGULATOR

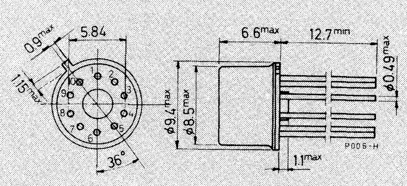
- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING

The L123 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic package and 10-lead Metal Can (TO-100 type). The circuit provides internal current limiting. When the output current excedes 150 mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

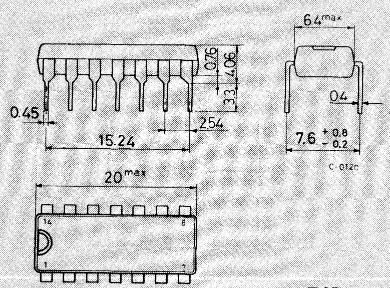
ABSOLUTE MAXIMUM RATINGS		L123	L123 C
V_i	Input voltage	40 V	40 V
ΔV_{i-o}	Dropout voltage	40 V	40 V
I_o	Output current	150 mA	150 mA
I_{ref}	Current from V_{ref}	15 mA	25 mA
P_{tot}	Power dissipation (at $T_{amb} = 70°C$) Plastic DIP	–	1 W
	TO-100	520 mW	520 mW
T_{op}	Operating junction temperature	-25 to 150 °C	0 to 70 °C
T_{stg}	Storage temperature	-65 to 150 °C	-65 to 150 °C

MECHANICAL DATA

Dimensions in mm

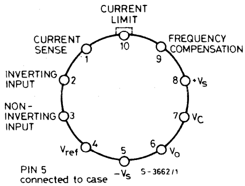


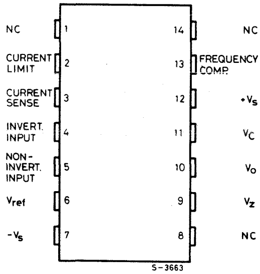
TO-100



DIP

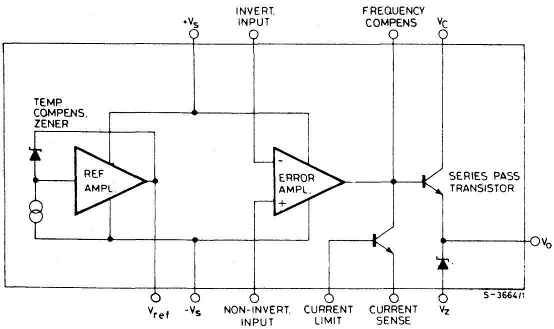
CONNECTION DIAGRAM AND ORDERING NUMBERS
(top views)



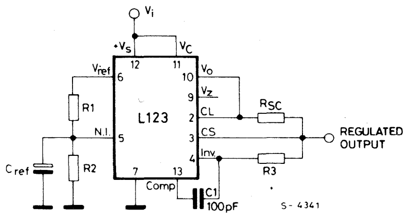


Type	TO-100	Plastic DIP
L123	L123TB	–
L123C	L123CTB	L123CB

BLOCK DIAGRAM



TEST CIRCUIT
(Pin configuration relative to the Plastic package)



V_i = 12V
V_o = 5V
I_o = 1 mA
$R_1 // R_2 \leqslant 10\ K\Omega$

THERMAL DATA		TO-100	Plastic DIP
$R_{th\ j\text{-}amb}$ Thermal resistance junction-ambient	max	155 °C/W	80 °C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	L123C Min.	L123C Typ.	L123C Max.	L123 Min.	L123 Typ.	L123 Max.	Unit
$\frac{\Delta V_o}{\Delta V_i}$	Line regulation	V_i = 12 to 15V		0.01	0.1		0.01	0.1	%
		V_i = 12 to 40V		0.1	0.5		0.02	0.2	%
		V_i = 12 to 15V; $T_{min} \leq T_{amb} \leq T_{max}$			0.3			0.3	%
$\frac{\Delta V_o}{V_o}$	Load regulation	I_o = 1 to 50 mA		0.03	0.2		0.03	0.15	%
		$T_{min} \leq T_{amb} \leq T_{max}$ I_o = 1 to 10 mA			0.6			0.6	%
V_{ref}	Reference voltage	I_{ref}= 160 µA	6.8	7.15	7.5	6.95	7.15	7.35	V
SVR	Ripple rejection	f = 100 Hz to 10 KHz C_{ref}= 0		74			74		dB
		C_{ref}= 5 µF		86			86		dB
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				150			150	$\frac{ppm}{°C}$
I_{sc}	Short circuit current limiting	R_{sc}= 10Ω V_o= 0		65			65		mA
V_i	Input voltage range		9.5		40	9.5		40	V
V_o	Output voltage range		2		37	2		37	V
V_i-V_o			3		38	3		38	V
I_d	Quiescent drain current	I_o = 0 V_i = 30V		2.3	4		2.3	5	mA
	Long term stability			0.1			0.1		$\frac{\%}{1000\ hrs}$
e_N	Output noise voltage	BW= 100 Hz to 10 KHz C_{ref}= 0		20			20		µV
		C_{ref}= 5 µF		2.5			2.5		µV
V_z	Output zener voltage (for plastic package only)	I_z = 1 mA	6.9		7.7				V

Note: T_{min} = 0°C (L123C); -25°C (L123).
T_{max}= 70°C (L123C); 150°C (L123).

Fig. 1 - Maximum output current vs. voltage drop

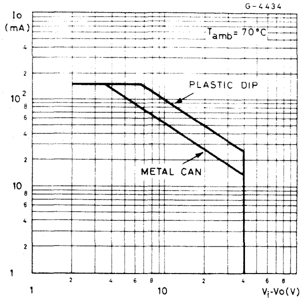


Fig. 2 - Current limiting characteristics

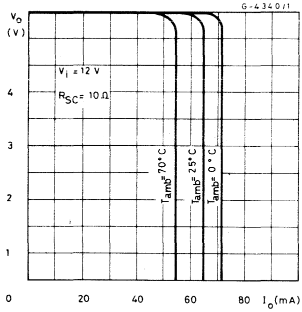


Fig. 3 - Current limiting characteristics vs. junction temperature

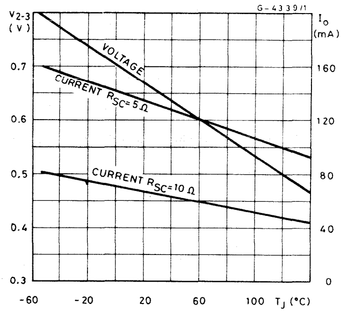


Fig. 4 - Load regulation characteristics without current limiting

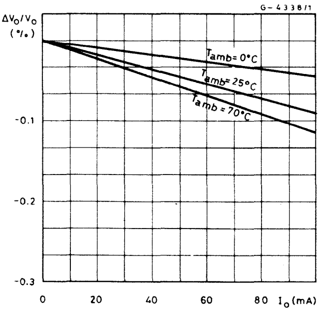


Fig. 5 - Load regulation characteristics with current limiting

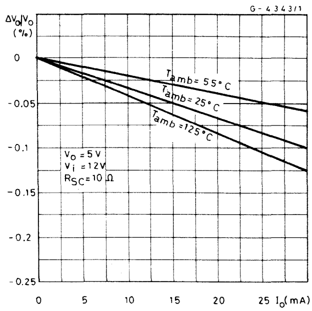


Fig. 6 - Load regulation characteristics with current limiting

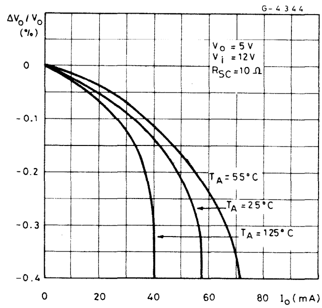


Fig. 7 - Line regulation vs. voltage drop

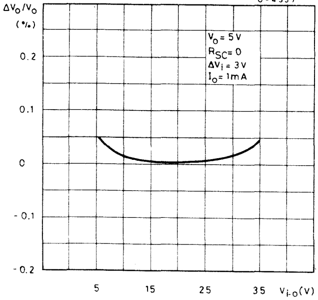


Fig. 8 - Load regulation vs. voltage drop

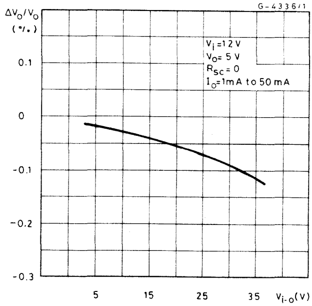


Fig. 9 - Quiescent drain current vs. input voltage

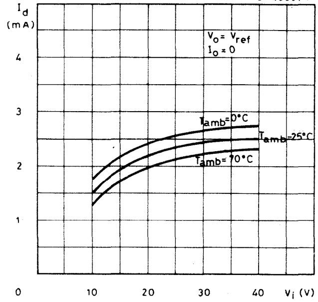


Fig. 10 - Line transient response

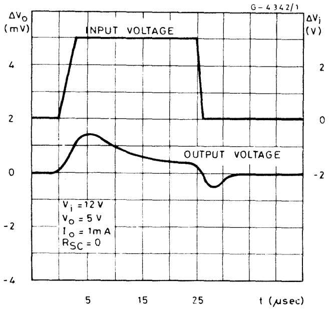


Fig. 11 - Load transient response

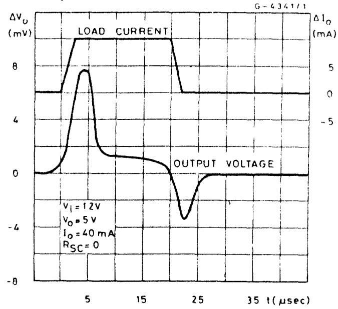


Fig. 12 - Output impedance vs. frequency

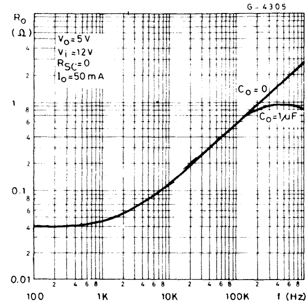


Table I — Resistor values (KΩ) for standard output voltages

Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)			Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	13, 16, 17 18, 21, 23	4.12	3.01	1.8	0.5	1.2	+100	19	3.57	102	2.2	10	91
+ 5	13, 16, 17 18, 21, 23	2.15	4.99	0.75	0.5	2.2	+250	19	3.57	255	2.2	10	240
+ 6	13, 16, 17 18, 21, 23	1.15	6.04	0.5	0.5	2.7	- 6(°°)	15	3.57	2.43	1.2	0.5	0.75
+ 9	14, 16, 17 18, 21, 23	1.87	7.15	0.75	1	2.7	- 9	15	3.48	5.36	1.2	0.5	2
+12	14, 16, 17 18, 21, 23	4.87	7.15	2	1	3	- 12	15	3.57	8.45	1.2	0.5	3.3
+15	14, 16, 17 18, 21, 23	7.87	7.15	3.3	1	3	- 15	15	3.65	11.5	1.2	0.5	4.3
+28	14, 16, 17 18, 21, 23	21	7.15	5.6	1	2	- 28	15	3.57	24.3	1.2	0.5	10
+45	19	3.57	48.7	2.2	10	39	- 45	20	3.57	41.2	2.2	10	33
+75	19	3.57	78.7	2.2	10	68	-100	20	3.57	97.6	2.2	10	91
							-250	20	3.57	249	2.2	10	240

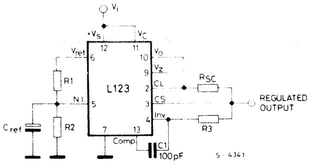
Note: (°) Replace R_1/R_2 divider with the circuit of fig. 24.
(°°) V^+ must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 13, 17, 18, 21, 23, 16 $V_O = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts Fig. 19 $V_O = [\frac{V_{ref}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 14, 16, 17, 18, 21, 23 $V_O = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from -6 to -250 volts Fig. 15, 20 $V_O = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_O\ R_3}{R_{sc}\ R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc}\ R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

APPLICATION INFORMATION (Pin numbers relative to the plastic package)

Fig. 13 - Basic low voltage regulator (V_o = 2 to 7V)

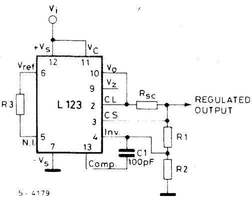


NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance
Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) . . . . . . .0.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .1.5 mV

Fig. 14 - Basic high voltage regulator (V_o = 7 to 37V)

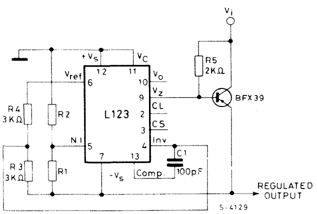


NOTE: $\frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

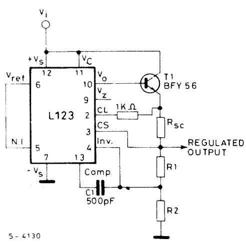
Typical performance
Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . . .1.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .4.5 mV

Fig. 15 - Negative voltage regulator



Typical performance
Regulated Output Voltage . . . .-15V
Line Regulation (ΔV_i = 3V) . . . . .1 mV
Load Regulation (ΔI_O = 100 mA) . . . .2 mV

Fig. 16 - Positive voltage regulator (External NPN Pass Transistor)



Typical performance
Regulated Output Voltage . . . .+15V
Line Regulation (ΔV_i = 3V) . . . . . . .1.5 mV
Load Regulation (ΔI_O = 1A) . . . . . . 15 mV

APPLICATION INFORMATION (continued)

Fig. 17 – Positive voltage regulator (External PNP Pass Transistor)

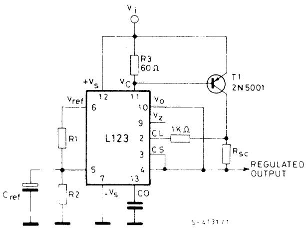
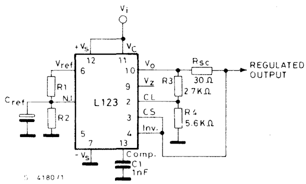


Fig. 18 – Foldback current limiting



Typical performance
Regulated Output Voltage . . . . +5V
Line Regulation ($\Delta V_i = 3V$) . . . . 0.5 mV
Load Regulation ($\Delta I_O = 1A$) . . . . 5 mV

Typical performance
Regulated Output Voltage . . . . +5V
Line Regulation ($\Delta V_i = 3V$) . . . . 0.5 mV
Load Regulation ($\Delta I_O = 10$ mA) . . . . . 1 mV
Current Limit Knee . . . . 20 mA

Fig. 19 – Positive floating regulator

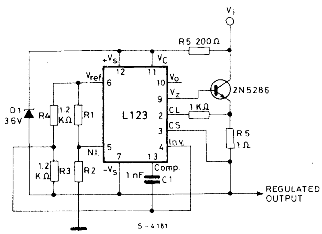
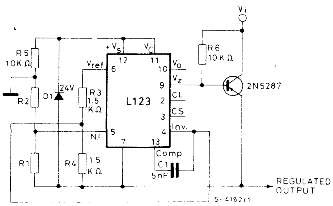


Fig. 20 – Negative floating regulator

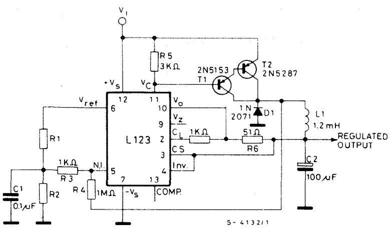


Typical performance
Regulated Output Voltage . . . . +100V
Line Regulation ($\Delta V_i = 20V$) . . . . . . 15 mV
Load Regulation ($\Delta I_O = 50$ mA) . . . . 20 mV

Typical performance
Regulated Output Voltage . . . . -100V
Line Regulation ($\Delta V_i = 20V$) . . . . . . 30 mV
Load Regulation ($\Delta I_O = 100$ mA) . . . 20 mV

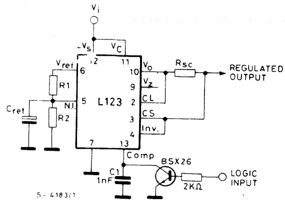
APPLICATION INFORMATION (continued)

Fig. 21 - Positive switching regulator



Typical performance
Regulated Output voltage . . . .+5V
Line Regulation ($\Delta V_i = 30V$) . . . . . . 10 mV
Load Regulation ($\Delta I_O = 2A$) . . . . . . 80 mV

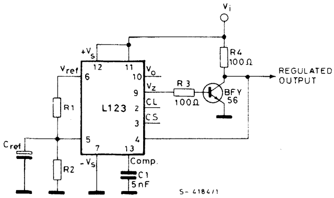
Fig. 22 - Remote shutdown regulator with current limiting



Typical performance
Regulated Output Voltage . . . .+5V
Line Regulation ($\Delta V_i = 3V$) . . . . . . .0.5 mV
Load Regulation ($\Delta I_O = 50$ mA) . . . .1.5 mV

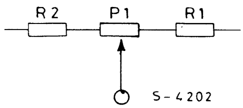
NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

Fig. 23 - Shunt regulator



Typical performance
Regulated Output Voltage . . . .+5V
Line Regulation ($\Delta V_i = 10V$) . . . . . . .2 mV
Load Regulation ($\Delta I_O = 100$ mA) . . . .5 mV

Fig. 24 - Output voltage adjust



L146
L146C

LINEAR INTEGRATED CIRCUITS

HIGH PRECISION HIGH VOLTAGE REGULATOR

- INPUT VOLTAGE UP TO 80V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 77V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT UP TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING
- THERMAL PROTECTION

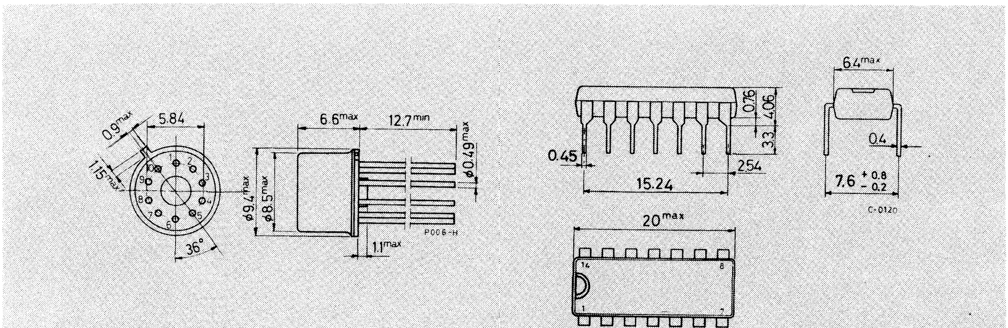
The L146 is a monolithic integrated programmable voltage regulator in 14-lead dual in-line plastic package and 10-lead Metal Can (TO-100 type). It is made with high voltage technology and provides internal current limiting and thermal shut down protection; when current exceeds 150 mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut down. **The L146 is intended to widen the application range of L123 up to 80V.**

ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage	80	V
V_i-V_o	Voltage drop	78	V
I_o	Output current	150	mA
I_{ref}	Current from V_{ref}	8	mA
P_{tot}	Power dissipation (at T_{amb}= 70°C) Plastic DIP	1	W
	TO-100	520	mW
T_{op}	Operating junction temperature L146	-25 to + 85	°C
	L146C	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

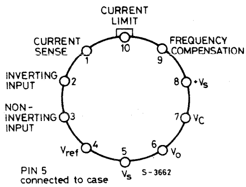
MECHANICAL DATA

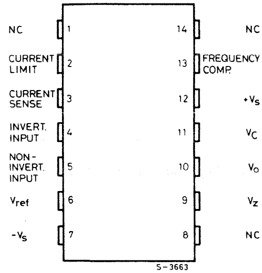
Dimensions in mm



TO-100 DIP

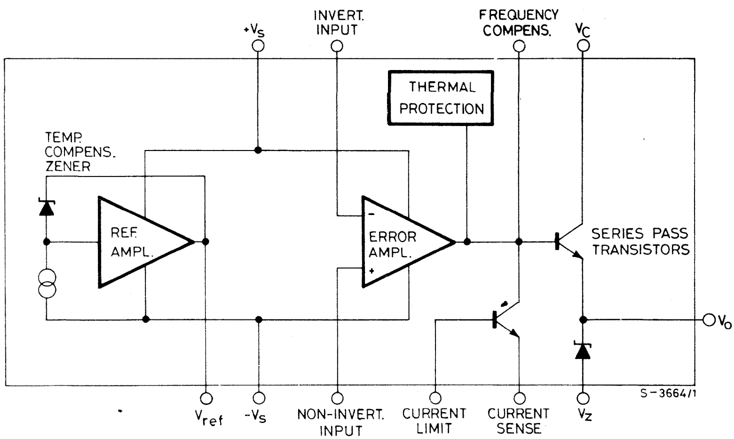
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top view)





Type	TO-100	Plastic DIP
L146	L146 TB	
L146 C	L146 CTB	L146 CB

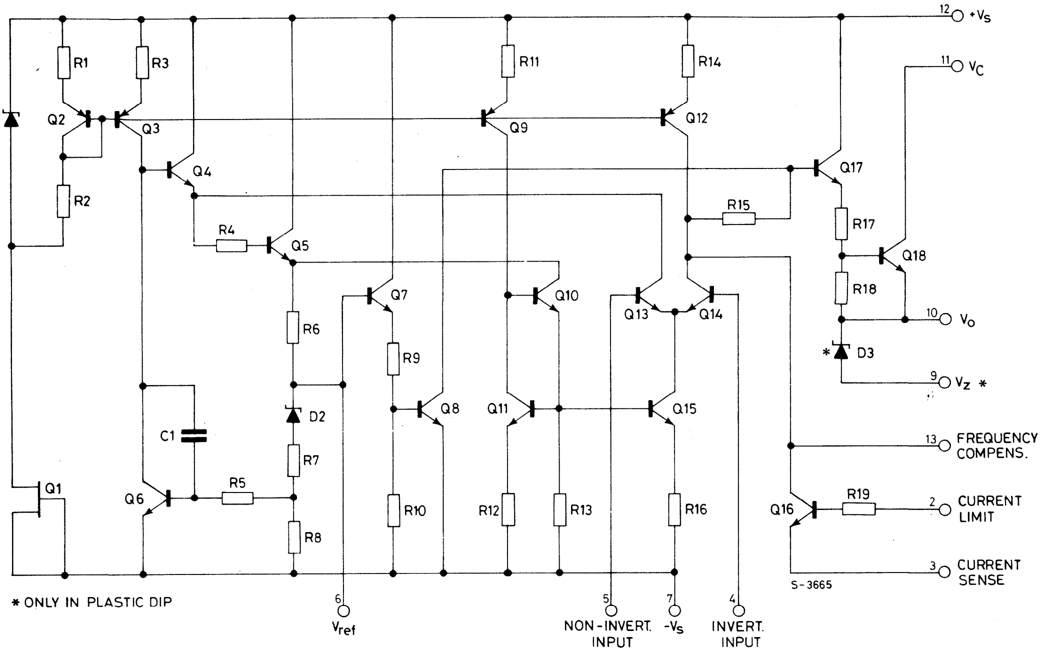
BLOCK DIAGRAM



THERMAL DATA

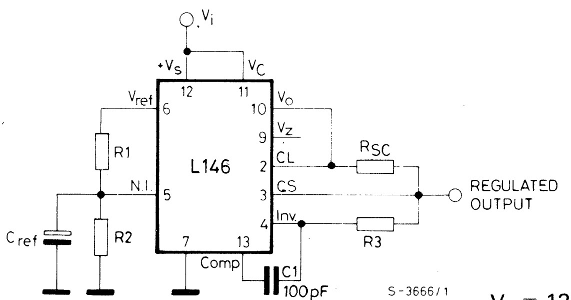
			TO-100	Plastic DIP
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155°C/W	80°C/W

SCHEMATIC DIAGRAM (pin number relative to the plastic package)



* ONLY IN PLASTIC DIP

TEST CIRCUIT



$V_i = 12V$
$V_o = 5V \quad I_o = 1\ mA$
$R_1 // R_2 \leqslant 10\ K\Omega$

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	L146 C Min.	L146 C Typ.	L146 C Max.	L146 Min.	L146 Typ.	L146 Max.	Unit
$\frac{\Delta V_o}{V_o}$	Line regulation	V_i = 12 to 15V V_i = 12 to 40V V_i = 40 to 80V		0.05 0.1 0.1	0.15 0.5 0.5		0.05 0.1 0.1	0.15 0.2 0.2	%
$\frac{\Delta V_o}{V_o}$	Load regulation	V_i = 12V V_o = 5V I_o = 1 to 50 mA		0.03	0.2		0.03	0.15	%
		V_i = 40V V_o = 37V I_o = 1 to 10 mA		0.1	0.5		0.1	0.3	%
		V_i = 80V V_o = 77V I_o = 1 to 10 mA		0.12	0.8		0.12	0.5	%
V_{ref}	Reference voltage	I_{ref} = 160 μA	7.75	8.15	8.55	7.9	8.15	8.4	V
ΔV_{ref}		I_{ref} = 160 μA to 5 mA		4	14		4	14	mV
SVR	Ripple rejection	f = 100 Hz to 10 KHz C_{ref} = 0 C_{ref} = 5 μF		60 88			60 88		dB
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				150			150	$\frac{ppM}{°C}$
I_{sc}	Short circuit current limiting	R_{sc} = 10Ω V_o = 0	50	60	70	50	60	70	mA
V_i	Input voltage range		10		80	10		80	V
V_o	Output voltage range		2		77	2		77	V
$V_i - V_o$	Voltage drop		3		78	3		78	V
I_d	Quiescent drain current	I_o = 0 V_o = 5V (including I_{ref} = 160 μA) V_i = 12V V_i = 40V V_i = 80V		4 5.6 6	5.5 7 7.5		4 5.6 6	5.5 7 7.5	mA
ΔI_d	Quiescent drain current change	I_o = 1 mA, V_o = 5V; V_i = 12 to 40V			2.2			1.6	mA
		I_o = 1 mA, V_o = 5V; V_i = 12 to 80V			2.6			2	mA
	Long term stability			0.1			0.1		$\frac{\%}{1000\ hrs}$
e_N	Output noise voltage	BW = 100 Hz to 10 KHz C_{ref} = 0 C_{ref} = 5 μF		300 30			300 30		μV
V_z	Output zener voltage (for plastic package only)	I_z = 1 mA	6.9		7.7				V

Fig. 1 - Maximum output current vs. voltage drop

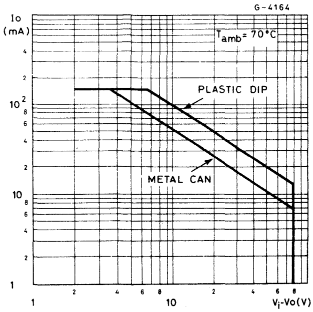


Fig. 2 - Load regulation vs. output current (with current limiting)

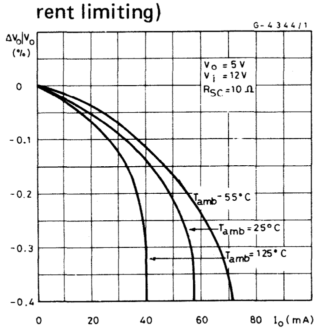


Fig. 3 - Load regulation vs. output current (with current limiting)

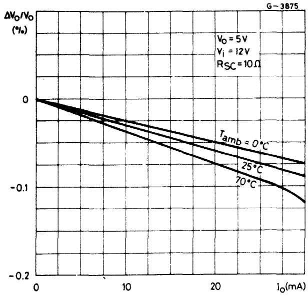


Fig. 4 - Load regulation vs. output current (without current limiting)

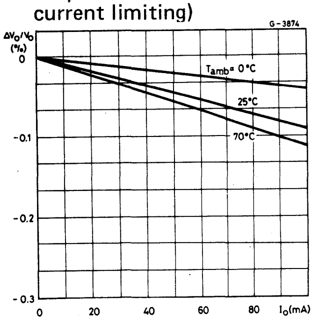


Fig. 5 - Current limiting characteristics

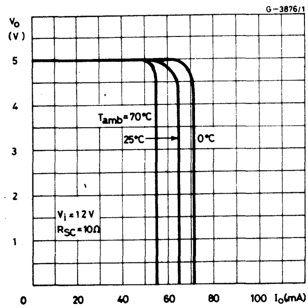


Fig. 6 - Current limiting characteristics vs. junction temperature

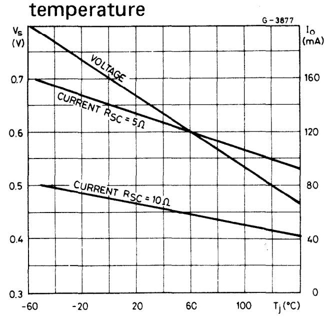


Fig. 7 - Line transient response

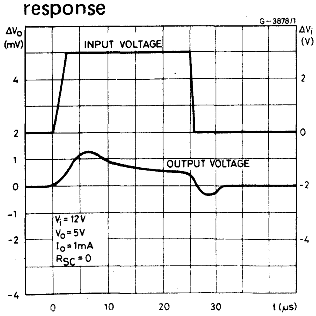


Fig. 8 - Load transient response

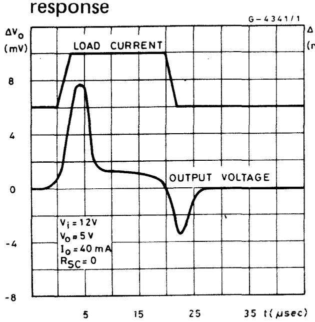


Fig. 9 - Output impedance vs. frequency

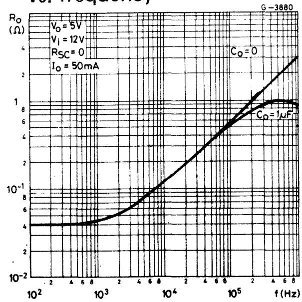


Table I — Resistor values (KΩ) for standard output voltage

Positive output voltage	Applicable figures	Fixed output ± 5%	
		R_1	R_2
+6	10, 13, 14 18, 20	2.4	6.8
+12	11, 13, 14, 15, 18, 20	3.2	6.8
+30		15	5.6
+50		24	47
+70		30	39
+100	16	2.7	68
+250		4.7	120

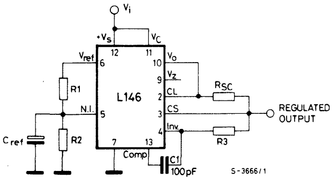
Negative output voltage	Applicable figures	Fixed output ± 5%	
		R_1	R_2
-9	12	2.2	2.7
-12		1.5	3
-30		4.7	30
-50		2.7	30
-100	17	2	47
-250		2	120

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 10, 13, 14, 15, 18, 20 $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts Fig. 16 $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +77 volts Fig. 11, 13, 14, 15, 18, 20 $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Output from -6 to -250 volts Fig. 12, 17 $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT}\ R_3}{R_{sc}\ R_4} + \frac{V_{SENSE}\ (R_3 + R_4)}{R_{sc}\ R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

APPLICATION CIRCUITS (continued)

Fig. 10 - Basic low voltage regulator (V_{OUT} = 2 to 7V)



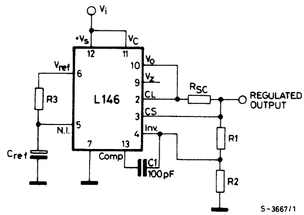
NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) . . . . . . .0.5 mV
Load Regulation (ΔI_o = 50 mA) . . . .1.5 mV

Fig. 11 - Basic high voltage regulator (V_{OUT} = 7 to 77V)



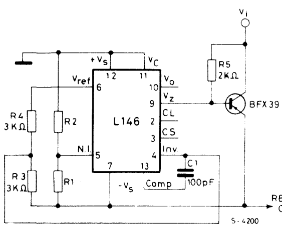
NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . . .1.5 mV
Load Regulation (ΔI_o = 50 mA) . . . .4.5 mV

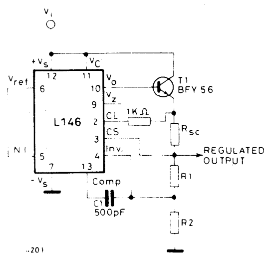
Fig. 12 - Negative voltage regulator



Typical performance

Regulated Output Voltage . . . .+15V
Line Regulation (ΔV_i = 3V) . . . . . . .1.5 mV
Load Regulation (ΔI_o = 1 A) . . . . . . 15 mV

Fig. 13 - Positive voltage regulator (External NPN Pass Transistor)

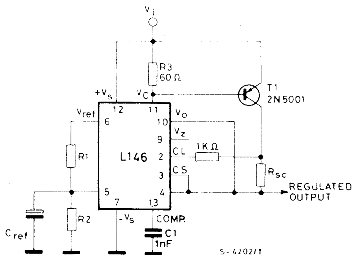


Typical performance

Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . .1 mV
Load Regulation (ΔI_o = 100 mA) . . . .2 mV

APPLICATION CIRCUITS (continued)

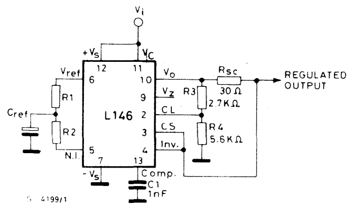
Fig. 14 - Positive voltage regulator (External PNP Pass Transistor)



Typical performance

Regulated Output Voltage . . . . +5V
Line Regulation ($\Delta V_i = 3V$) . . . . 0.5 mV
Load Regulation ($\Delta I_o = 1A$) . . . . 5 mV

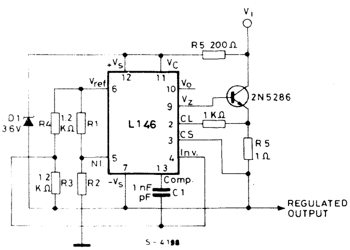
Fig. 15 - Foldback current limiting



Typical performance

Regulated Output Voltage . . . . +5V
Line Regulation ($\Delta V_i = 3V$) . . . . 0.5 mV
Load Regulation ($\Delta I_o = 10$ mA) . . . . . 1 mV
Current Limit Knee . . . . 20 mA

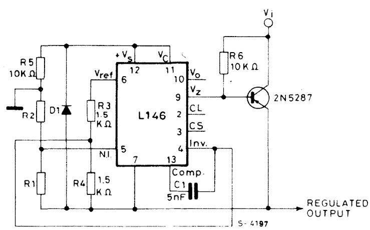
Fig. 16 - Positive floating regulator



Typical performance

Regulated Output Voltage . . . . +100V
Line Regulation ($\Delta V_i = 20V$) . . . . . . 15 mV
Load Regulation ($\Delta I_o = 50$ mA) . . . . 20 mV

Fig. 17 - Negative floating regulator

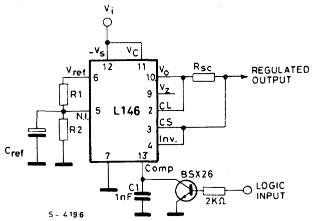


Typical performance

Regulated Output Voltage . . . . -100V
Line Regulation ($\Delta V_i = 20V$) . . . . . . 30 mV
Load Regulation ($\Delta I_o = 100$ mA) . . . 20 mV

APPLICATION CIRCUITS (continued)

Fig. 18 - Remote shutdown regulator with current limiting

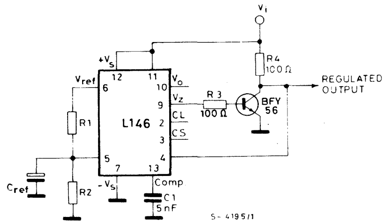


Typical performance

Regulated Output Voltage 5V
Line Regulation ($\Delta V_i = 3V$) 0.5V
Load Regulation ($\Delta I_o = 50$ mA) . . . .1.5 mV

NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

Fig. 19 - Shunt regulator



TYPICAL PERFORMANCE

Regulated Output Voltage . . . .+5V
Line Regulation ($\Delta V_i = 10V$) . . . . . .2 mV
Load Regulation ($\Delta I_o = 100$ mA) 5mV

Fig. 20 - 60V voltage regulator with foldback characteristic

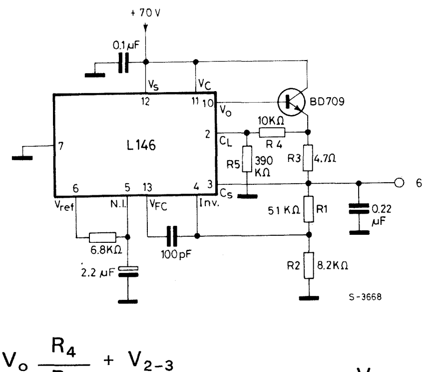
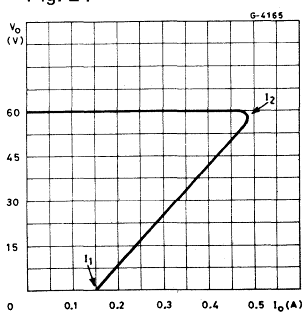


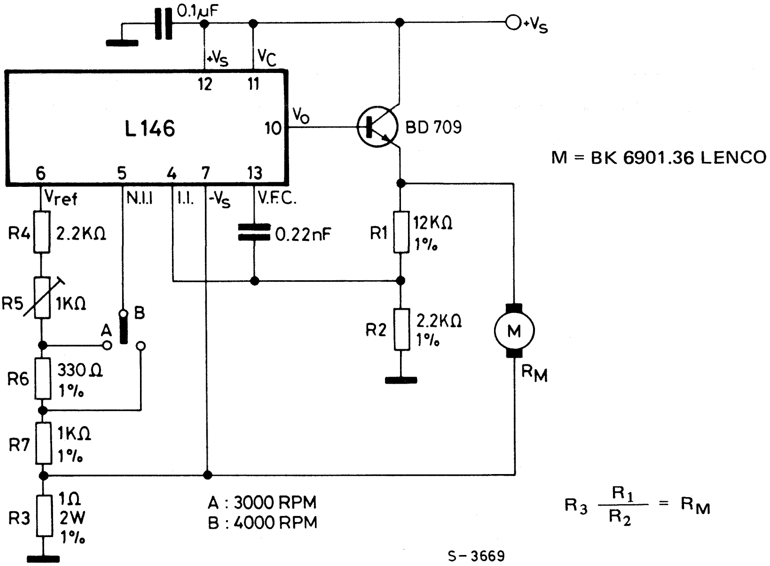
Fig. 21



$$I_2 = \frac{V_o \dfrac{R_4}{R_5} + V_{2-3}}{R_{SC}} \;; \qquad I_1 = \frac{V_{2-3}}{R_{SC}}\left(1 + \frac{R_4}{R_5}\right); \qquad V_{2-3} \cong 0.7V$$

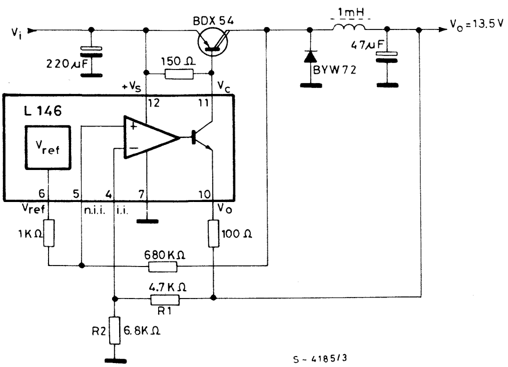
APPLICATION CIRCUITS (continued)

Fig. 22 - Motor speed control



$$R_3 \frac{R_1}{R_2} = R_M$$

Fig. 23 - Step-down switching regulator for 12V car radio



Performance:

Output voltage	13.5V
Max output current	3A
Input voltage range	20 to 30V
Line regulation	50 dB (I_o= 2A) ΔV_i= 10V
Load regulation	0.1% (ΔI_o= 3A)
Ripple	100 mVpp
Efficiency	75% (I_o= 3A)
Switching frequency	25 KHz

SGS **L149**

LINEAR INTEGRATED CIRCUITS

4A LINEAR DRIVER

- HIGH OUTPUT CURRENT (4A peak)
- HIGH CURRENT GAIN (10 000 TYP.)
- OPERATION UP TO ± 20V
- THERMAL PROTECTION
- SHORT CIRCUIT PROTECTION
- OPERATION WITHIN SOA
- HIGH SLEW-RATE (30V/μs)

The L149 is a general purpose power booster in PENTAWATT package consisting of a quasi-complementary darlington output stage with the associated biasing system and inhibit facility.
The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current.

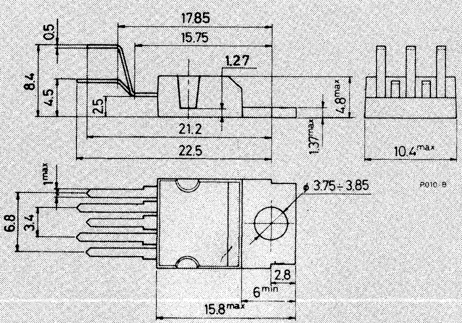
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	±20	V
V_i	Input voltage	V_s	
I_o	DC output current	3	A
I_o	Peak output current (internally limited)	4	A
V_{INH}	Input inhibit voltage	$-V_s +5$	V
		$-V_s - 1.5$	V
P_{tot}	Power dissipation at $T_{case} = 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

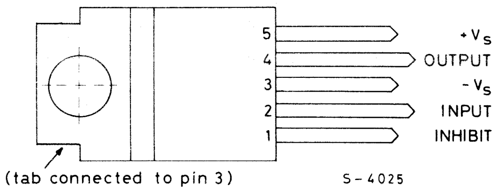
ORDERING NUMBER: L149V

MECHANICAL DATA

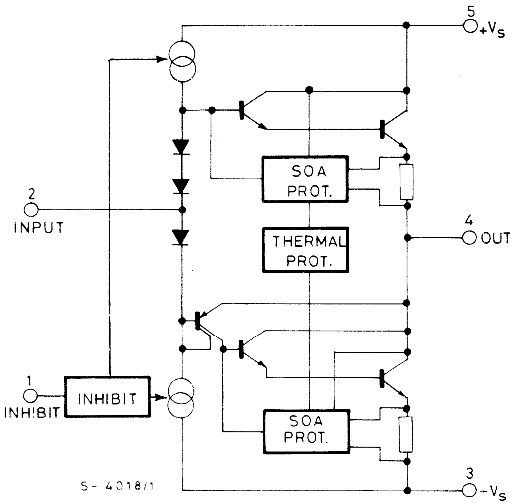
Dimensions in mm



CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage				± 20	V
I_d	Quiescent drain current	V_s = ± 16V		30		mA
I_{in}	Input current	V_s = ± 16V V_i = 0V		200	400	μA
h_{FE}	DC current gain	V_s = ± 16V I_o = 3A	6000	10000		–
G_v	Voltage gain	V_s = ± 16V I_o = 1.5A		1		–
V_{CEsat}	Saturation voltage (for each transistor)	I_o = 3A			3.5	V
V_{os}	Input offset voltage	V_s = ± 16V			0.3	V
V_{INH}	Inhibit input voltage (pins 1–3)	ON condition			± 0.3	V
		OFF condition	± 1.2			V
R_{INH}	Inhibit input resistance	f = 1 KHz		2.0		KΩ
SR	Slew rate			30		V/μs
B	Power bandwidth	V_s= ±18V, d = 1%, R_L= 8Ω		200		KHz

TEST CIRCUIT

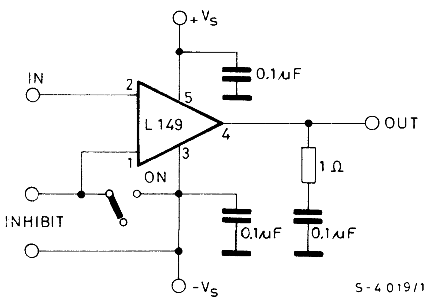


Fig. 1 - Maximum saturation voltage vs. output current

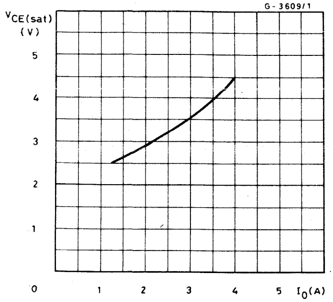


Fig. 2 - Current limiting characteristics

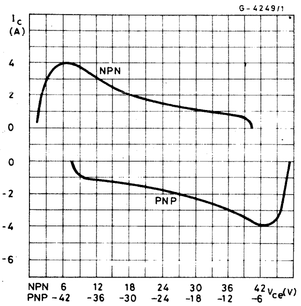
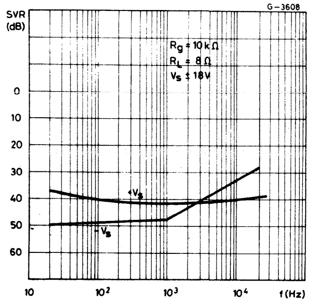


Fig. 3 - Supply voltage rejection vs. frequency



APPLICATION INFORMATION

Fig. 4 - High slew-rate power operational amplifier

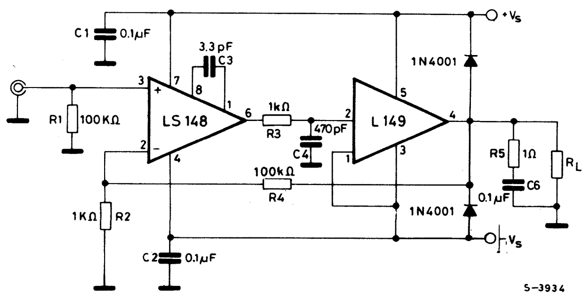


Fig. 5 - Distortion vs. output power (f = 1 KHz)

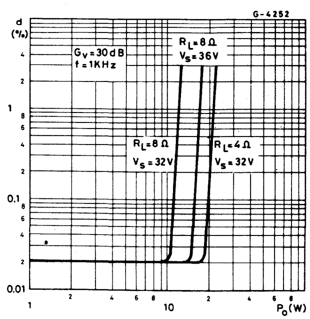


Fig. 6 - Distortion vs. output power (f= 10 KHz)

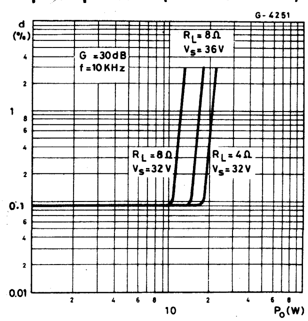
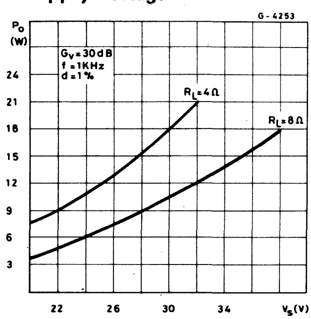


Fig. 7 - Output power vs. supply voltage



APPLICATION INFORMATION (continued)

Fig. 8 – Electronic potentiometer (short-circuit protected)

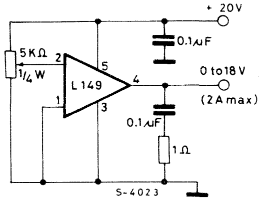
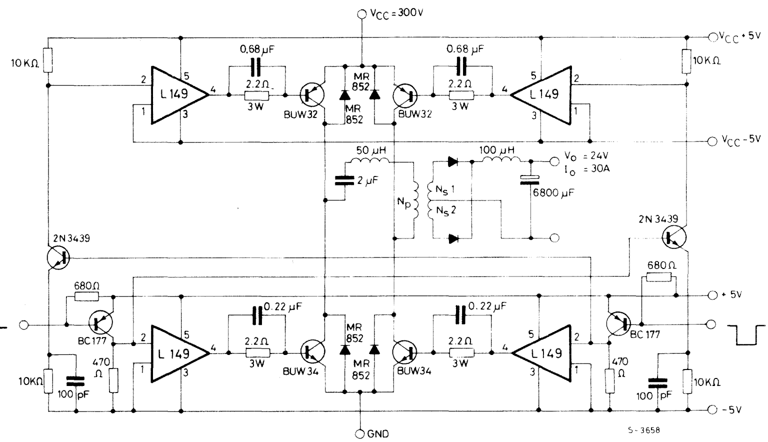


Fig. 9 – 720W Switch-Mode Power Supply using the L149 as driver stage for the power transistors



LINEAR INTEGRATED CIRCUITS

SGS **L165**

3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ±18V SUPPLY
- PENTAWATT PLASTIC PACKAGE

The L165 is a monolithic integrated circuit in PENTAWATT package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/ power booster combination is required.

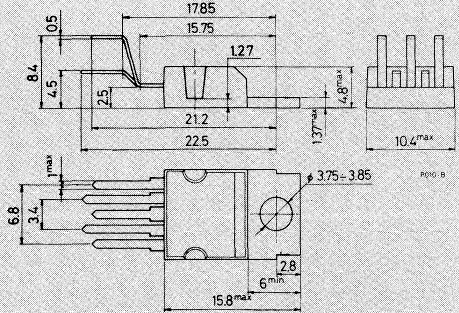
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: L165V

MECHANICAL DATA

Dimensions in mm



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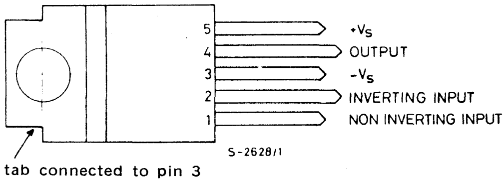
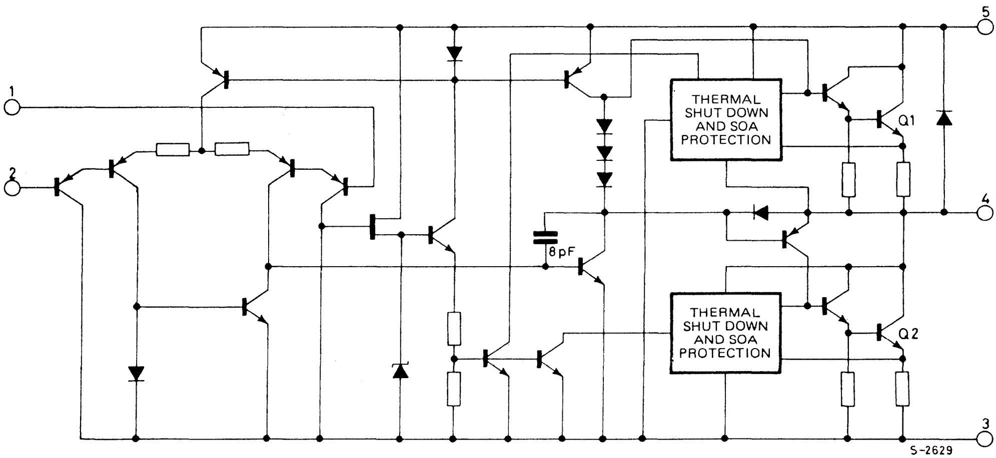
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		±18	V
I_d	Quiescent drain current	V_s = ± 18V		40	60	mA
I_b	Input bias current	V_s = ± 18V		0.2	1	μA
V_{os}	Input offset voltage	V_s = ± 18V		± 2	±10	mV
I_{os}	Input offset current	V_s = ± 18V		±20	±200	nA
SR	Slew-Rate	G_v = 10		8		V/μs
		G_v = 1 (°)		6		V/μs
V_o	Output voltage swing	f = 1 kHz, I_p = 0.3A I_p = 3A		27 24		V_{pp}
		f = 10 kHz, I_p = 0.3A I_p = 3A		27 23		V_{pp}
R_i	Input resistance (pin 1)	f = 1 KHz	100	500		KΩ
G_v	Voltage gain (open loop)	f = 1 KHz		80		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz		2		μV
i_N	Input noise current	B = 10 to 10 000 Hz		100		pA
CMR	Common mode rejection	R_g ≤ 10 KΩ G_v = 30 dB		70		dB
SVR	Supply voltage rejection	R_g = 22 kΩ, V_{ripple} = 0.5 V_{rms}, f_{ripple} = 100 Hz; G_v = 10		60		dB
		R_g = 22 kΩ, V_{ripple} = 0.5 V_{rms}, f_{ripple} = 100 Hz; G_v = 100		40		dB
η	Efficiency	f = 1 kHz, R_L = 4Ω; I_p = 1.6A; P_o = 5W		70		%
		f = 1 kHz, R_L = 4Ω; I_p = 3A; P_o = 18W		60		%
T_{sd}	Thermal shut-down case temperature	P_{tot} = 12W		110		°C
		P_{tot} = 6W		130		°C

(°) Circuit of fig. 8.

Fig. 1 - Open loop frequency response

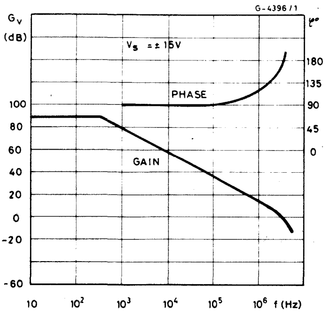


Fig. 2 - Closed-loop frequency response (circuit of fig. 8)

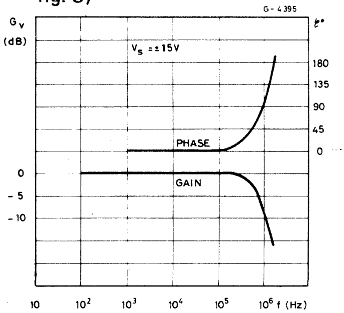


Fig. 3 - Large signal frequency response

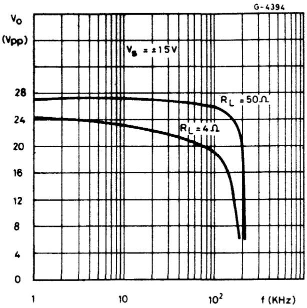


Fig. 4 - Maximum output current vs. voltage [V_{CE}] across each output transistor

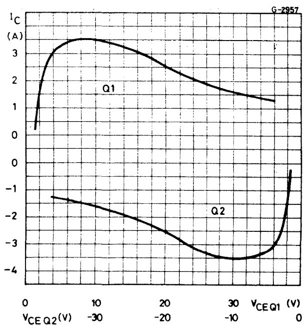


Fig. 5 - Safe operating area and collector characteristics of the protected power transistor

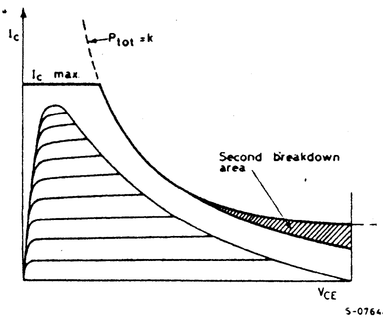


Fig. 6 - Maximum allowable power dissipation vs. ambient temperature

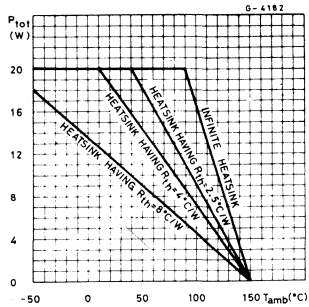


Fig. 7 - Application circuit ($G_V > 10$)

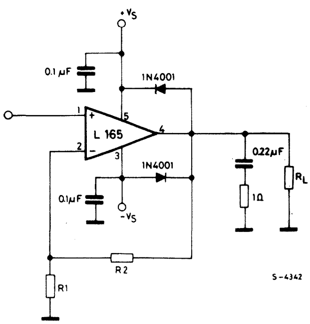


Fig. 8 - Unity gain configuration

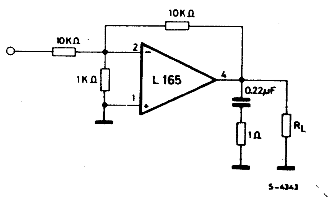
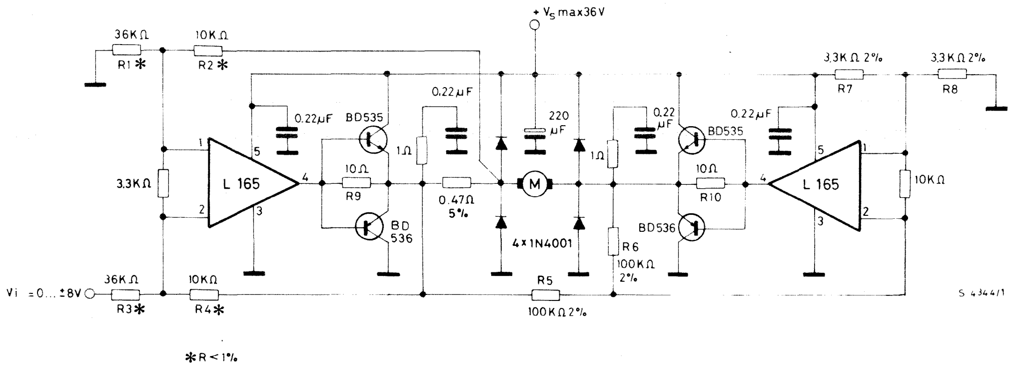
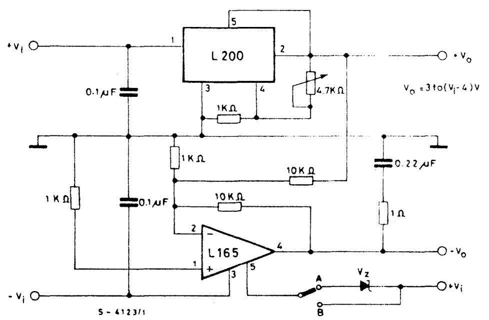


Fig. 9 - Motor current control circuit with external power transistors ($I_{motor} > 3.5A$)



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 10 - High current tracking regulator



A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – V_z must be chosen in order to verify $2V_i - V_z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

Fig. 11 - Bidirectional speed control of DC motor

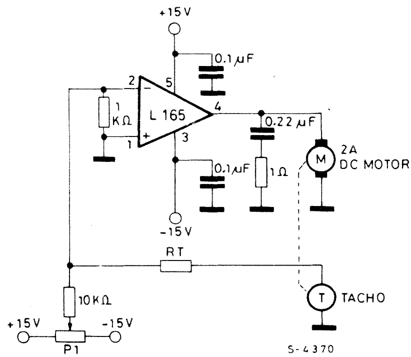


Fig. 12 - Split power supply

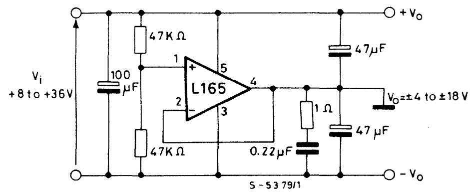
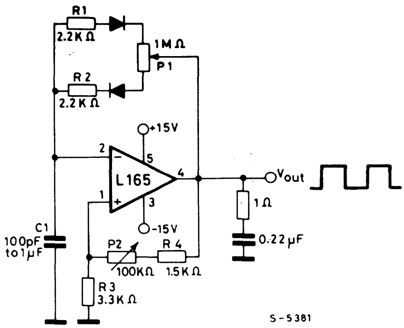
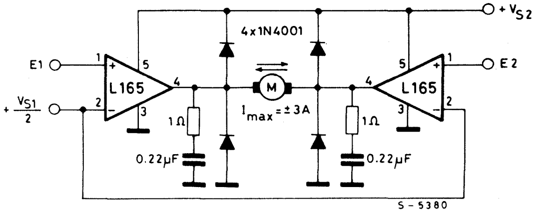


Fig. 13 - Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



P1 : duty-cycle adjust
P2 : frequency adjust (f = 700 Hz with C1= 10 nF, P2= 100 KΩ, f=25 Hz with C1= 10 nF, P2= 0)

Fig. 14 - Bidirectional DC motor control with TTL/C-MOS/µP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} \geqslant V_{S1}$

E1, E2 = logic inputs

LINEAR INTEGRATED CIRCUITS

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

- ADJUSTABLE OUTPUT CURRENT UP TO 2A (GUARANTEED UP TO $T_j = 150°C$)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

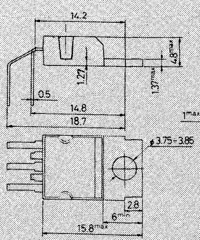
The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in PENTAWATT package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60V) make the L200 virtually blowout proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.

ABSOLUTE MAXIMUM RATINGS

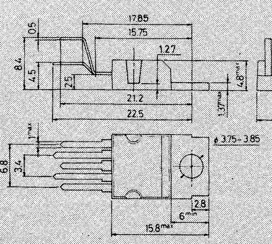
V_i	DC input voltage	40	V
V_i	Peak input voltage (10 ms)	60	V
ΔV_{i-o}	Dropout voltage	32	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature for L200C	-25 to 150	°C
	for L200	-55 to 150	°C

MECHANICAL DATA

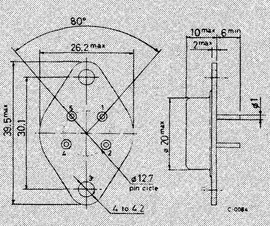
Dimensions in mm



Pentawatt H

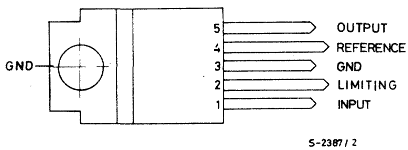


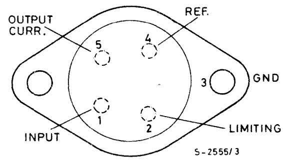
Pentawatt V



TO-3

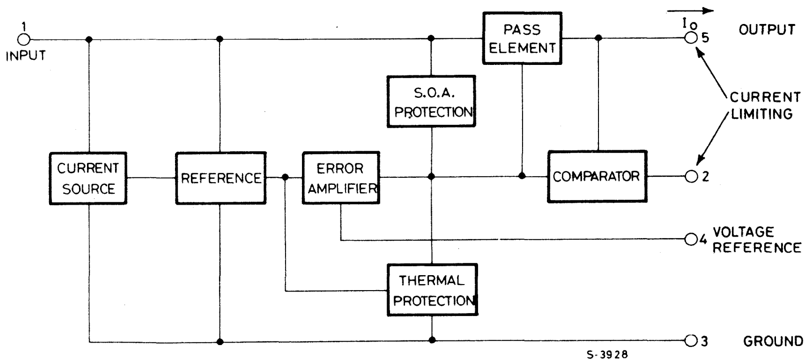
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



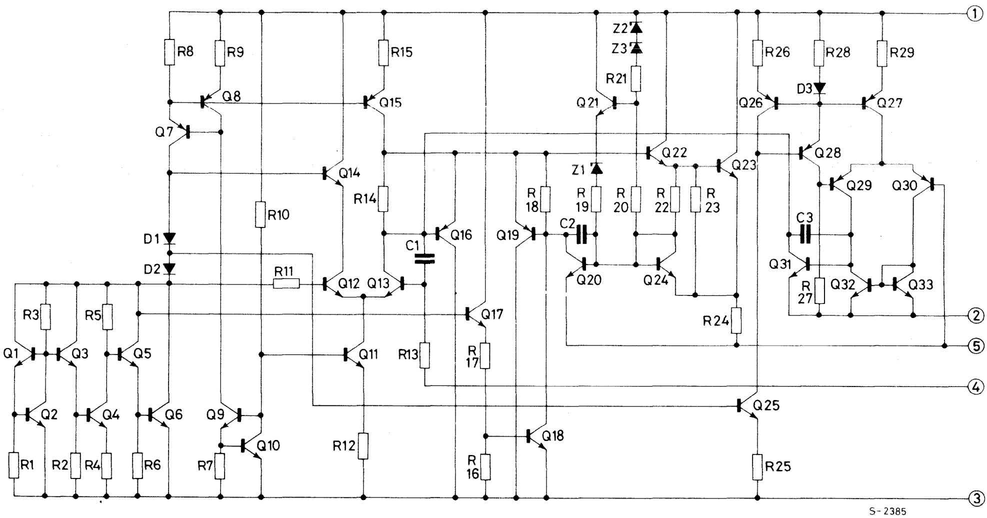


Type	Pentawatt®	TO-3
L 200		L 200 T
L 200 C	L 200 CH L 200 CV	L 200 CT

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	Pentawatt®
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent drain current (pin 3)	V_i = 20V		4.2	9.2	mA
e_N	Output noise voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		μV
V_o	Output voltage range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage load regulation (note 1)	ΔI_o = 2A ΔI_o = 1.5A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line regulation	V_o = 5V V_i = 8 to 18V	48	60		dB
SVR	Supply voltage rejection	V_o = 5V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
ΔV_{i-o}	Droupout voltage between pins 1 and 5	I_o = 1.5A $\Delta V_o \leqslant 2\%$		2	2.5	V
V_{ref}	Reference voltage (pin 4)	V_i = 20V I_o = 10 mA	2.64	2.77	2.86	V
ΔV_{ref}	Average temperature coefficient of reference voltage	V_i = 20V I_o = 10 mA for T_j= –25 to 125°C for T_j= 125 to 150°C		 -0.25 -1.5		 mV/°C mV/°C
I_4	Bias current at pin 4			3	10	μA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average temperature coefficient (pin 4)			-0.5		%/°C
Z_o	Output impedance	V_i = 10V V_o= V_{ref} I_o= 0.5A f = 100 Hz		1.5		mΩ

CURRENT REGULATION LOOP

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{SC}	Current limit sense voltage between pins 5 and 2	V_i = 10V V_o = V_{ref} I_5= 100 mA	0.38	0.45	0.52	V
$\frac{\Delta V_{sc}}{\Delta T \cdot V_{sc}}$	Average temperature coefficient of V_{SC}			0.03		%/°C
$\frac{\Delta I_o}{I_o}$	Current load regulation	V_i = 10V ΔV_o= 3V I_o = 0.5A I_o = 1A I_o = 1.5A		 1.4 1 0.9		 % % %
I_{sc}	Peak short circuit current	V_i - V_o = 14V (pins 2 and 5 short circuited)			3.6	A

Note 1): A load step of 2A can be applied provided that input-output differential voltage is lower than 20V (see fig. 1).

Note 2): The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Fig. 1 - Typical safe operating area protection

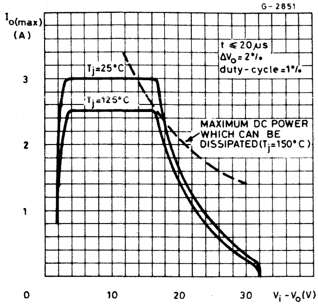


Fig. 2 - Quiescent current vs. supply voltage

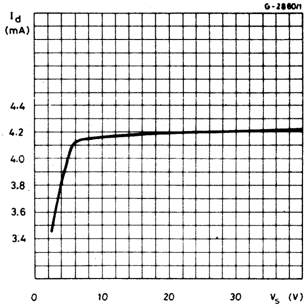


Fig. 3 - Quiescent current vs. junction temperature

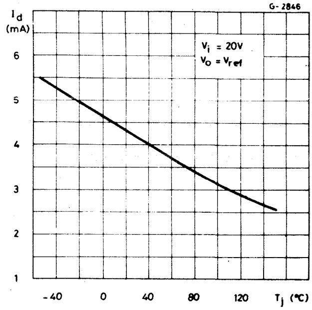


Fig. 4 - Quiescent current vs. output current

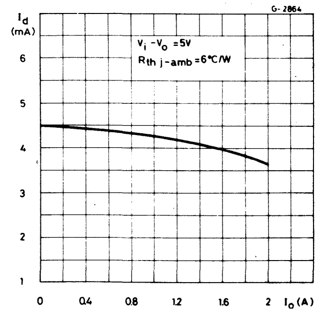


Fig. 5 - Output noise voltage vs. output voltage

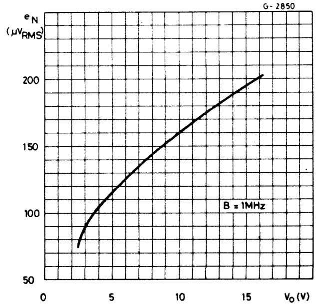


Fig. 6 - Output noise voltage vs. frequency

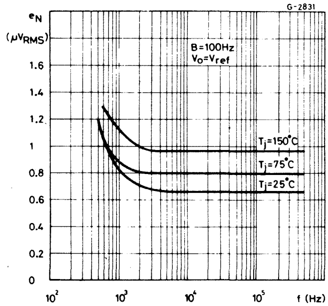


Fig. 7 - Reference voltage vs. junction temperature

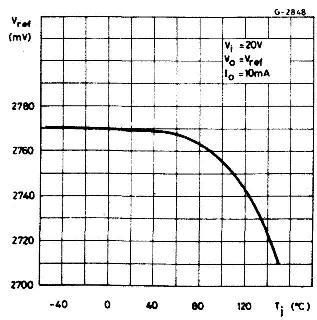


Fig. 8 - Voltage load regulation vs. junction temperature

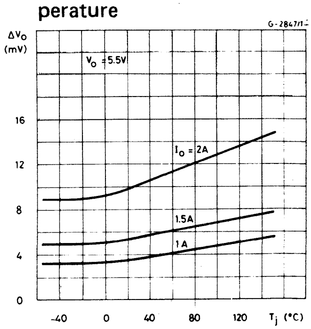


Fig. 9 - Supply voltage rejection vs. frequency

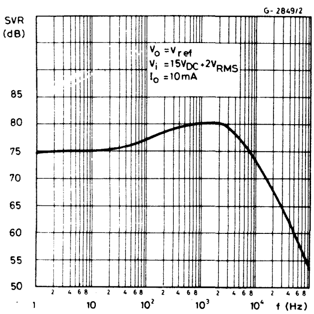


Fig. 10 - Dropout voltage vs. junction temperature

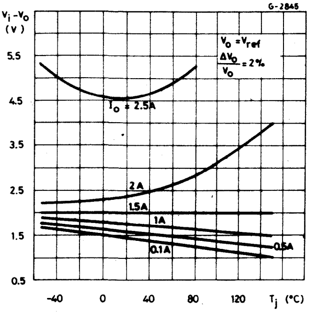


Fig. 11 - Output impedance vs. frequency

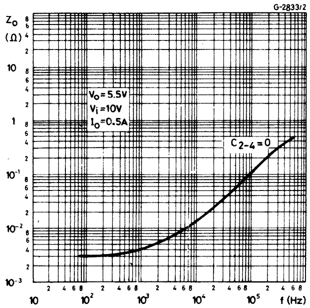


Fig. 12 - Output impedance vs. output current

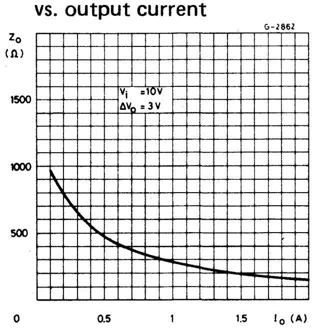


Fig. 13 - Voltage transient response

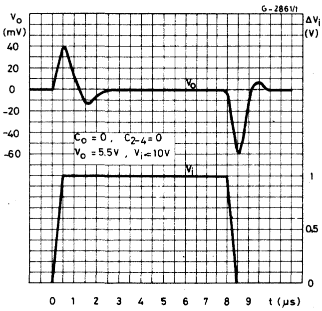


Fig. 14 - Load transient response

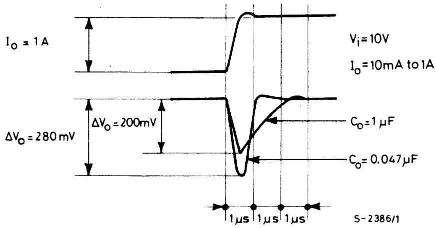


Fig. 15 - Load transient response

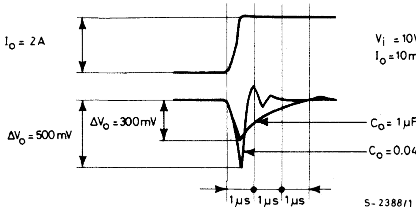
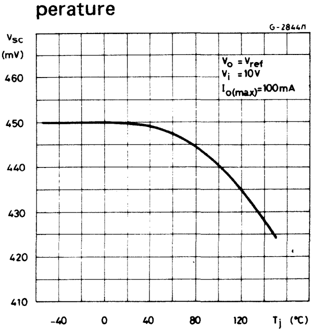


Fig. 16 - Current limit sense voltage vs. junction temperature



APPLICATION CIRCUITS

Fig. 17 – Programmable voltage regulator

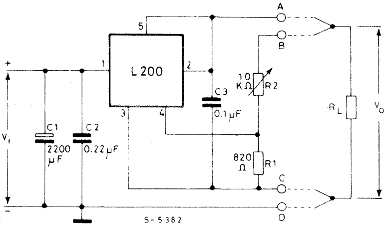


Fig. 18 – P.C. board and components layout of fig. 17. (1 : 1 scale)

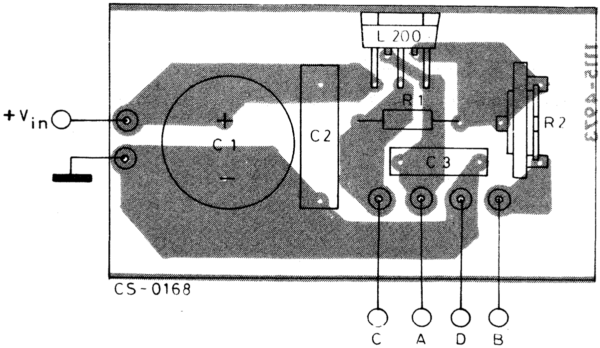


Fig. 19 – Programmable voltage regulator with current limiting

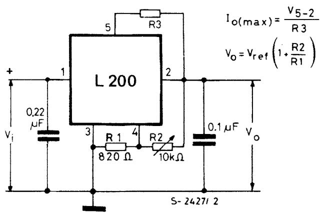


Fig. 20 – Programmable current regulator

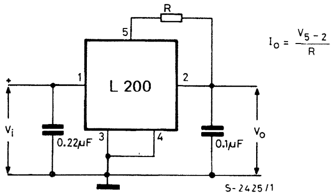


Fig. 21 – High current voltage regulator with short circuit protection

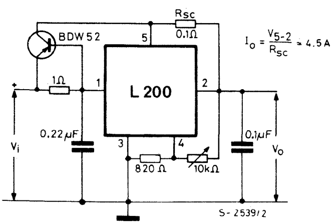
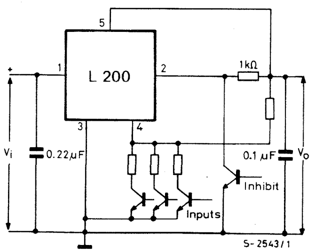
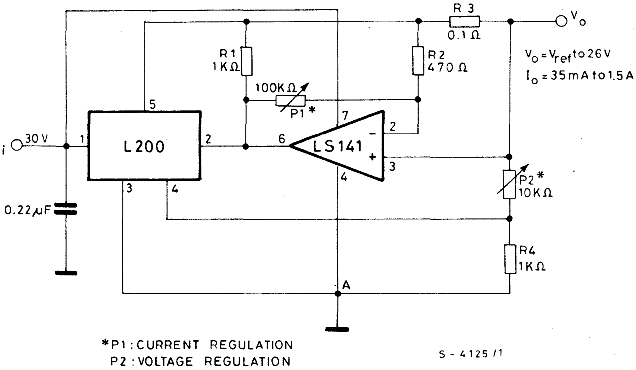


Fig. 22 – Digitally selected regulator with inhibit



APPLICATION CIRCUITS

Fig. 23 – Programmable voltage and current regulator



Note: Connecting point A to a negative voltage (for example-3V/10 mA) it is possible to extend the output voltage range down to 0V and to obtain the current limiting down to this level (output short-circuit condition).

Fig. 24 – High current regulator with NPN pass transistor

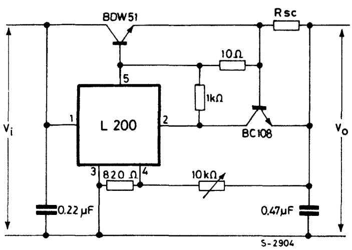
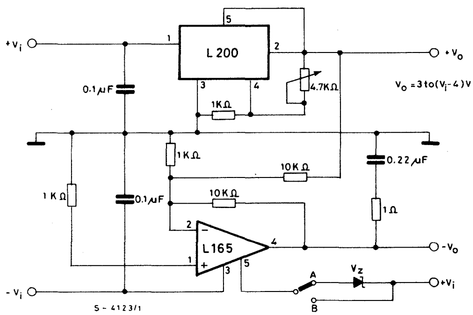


Fig. 25 – High current tracking regulator



A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – V_z must be chosen in order to verify $2V_i - V_z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

APPLICATION CIRCUITS (continued)

Fig. 26 – High input and output voltage

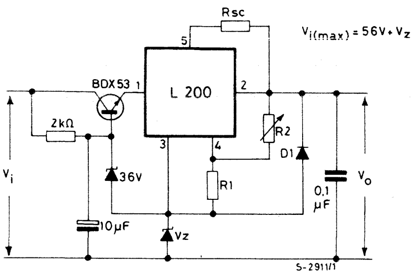
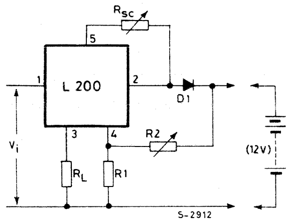
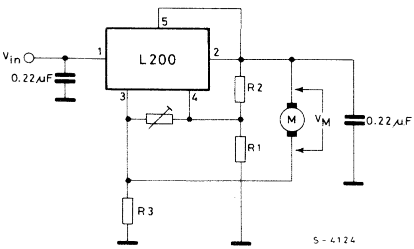


Fig. 27 – Constant current battery charger



The resistors R_1 and R_2 determine the final charging voltage and R_{sc} the initial charging current. D_1 prevents discharge of the battery throught the regulator.
The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12V/50 mA rating this will indicate incorrect connection.

Fig. 28 – 30W Motor speed control



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

Fig. 29 – Low turn on

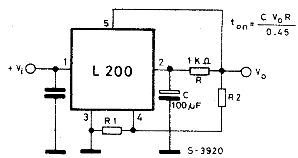
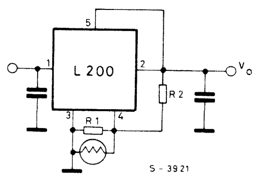


Fig. 30 – Light controller



L201 L202
L203 L204

LINEAR INTEGRATED CIRCUITS

DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA peak)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The L201, L202, L203 and L204 are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

L201	General purpose, DTL, TTL, PMOS, CMOS
L202	14-25V PMOS
L203	5V TTL, CMOS
L204	6 - 15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.
The L201, L202, L203 and L204 are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.

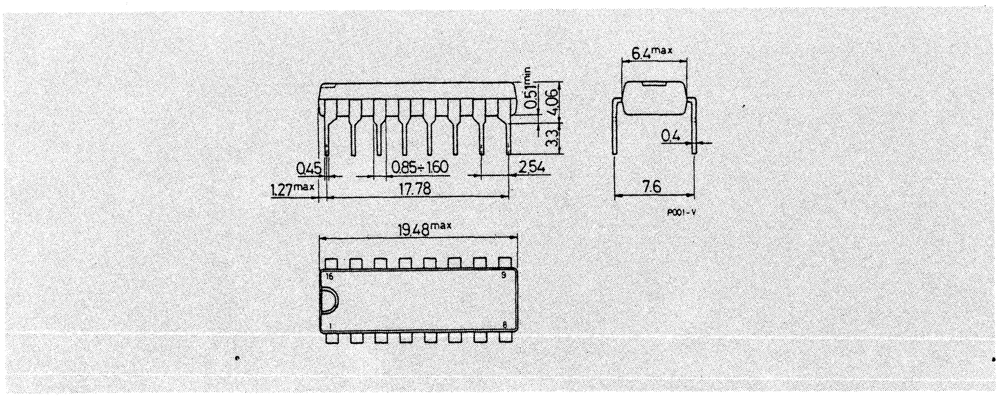
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (for **L 202, L 203** and **L 204**)	30	V
V_o	Output voltage (collector-emitter)	50	V
$V_{CEO(sus)}$	Collector-emitter sustaining voltage	36	V
I_C	Collector current	500	mA
I_B	Base current (for **L 201** only)	25	mA
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

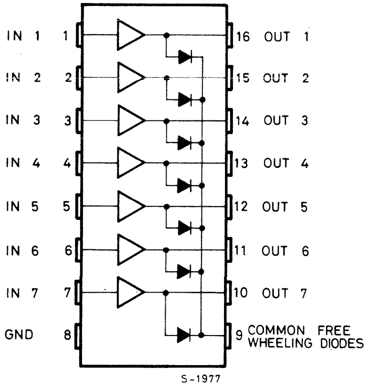
ORDERING NUMBERS: L201B-4, L203B-4
L202B-4, L204B-4

MECHANICAL DATA

Dimensions in mm

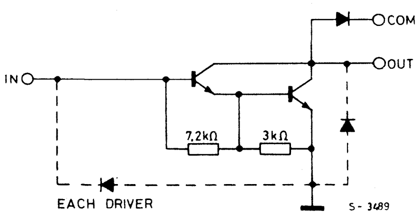


CONNECTION DIAGRAM (top view)

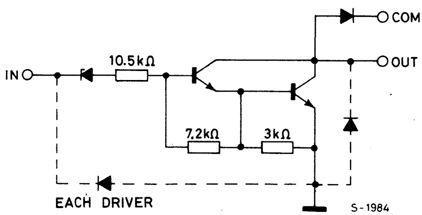


SCHEMATIC DIAGRAM

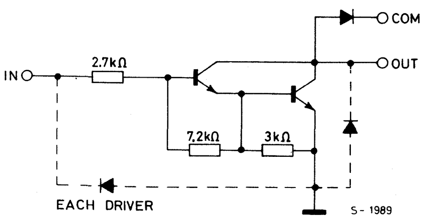
For L 201



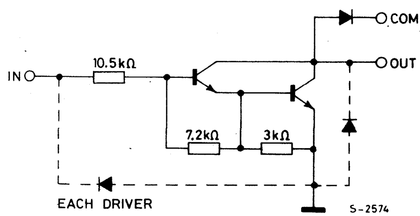
For L 202



For L 203



For L 204



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig. No.
I_{CEX}	Collector cutoff current	for **L 201** V_{CE} = 50V for **L 202** V_{CE} = 50V V_i = 7V for **L 203, L 204** V_{CE} = 50V I_i = 0		 0.2 0.2 0.2	 3 3 3	 μA μA μA	 1 2 1
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 350 mA I_B = 500 μA I_C = 200 mA I_B = 350 μA I_C = 100 mA I_B = 250 μA		1.25 1 0.85	1.6 1.3 1.1	V V V	3
I_i	Input current	for **L 202** V_i = 17V for **L 203** V_i = 3.85V for **L 204** V_i = 5V V_i = 12V		 0.75 0.9 0.35 1.1	 1.3 1.35 0.5 1.45	 mA mA mA mA	5
$I_{C(off)}$		V_{CE} = 50V I_i = 25 μA			25	μA	4
V_i	Input voltage	for **L 202** I_C = 300 mA V_{CE} = 2V for **L 203** I_C = 300 mA V_{CE} = 2V I_C = 250 mA V_{CE} = 2V for **L 204** V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 350 mA		 10.5 1.8 1.7 4.5 5	 13 3 2.4 6 8	 V V V V V	7
h_{FE}	DC current gain (for **L 201** only)	I_C = 350 mA V_{CE} = 2V	1000	3000		–	3
I_R	Parallel diode reverse current	V_R = 50V		0.5	50	μA	6
V_F	Parallel diode forward voltage	I_F = 350 mA		1.4	2	V	8
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o			5	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o			5	μs	–

TEST CIRCUITS

Fig 1 - For L 201, L 203 and L 204

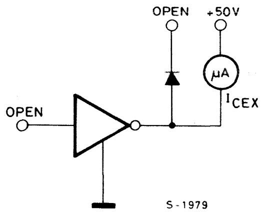


Fig. 2 - For L 202

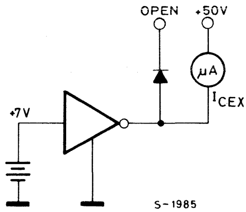


Fig. 3 - For L 201, L 202, L 203 and L 204

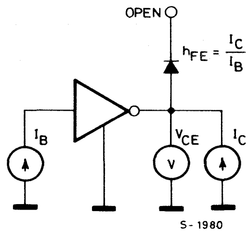


Fig. 4 - For L 201, L 202, L 203 and L 204

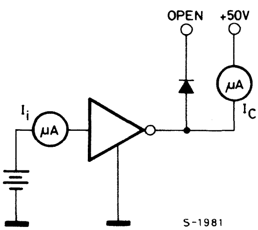


Fig. 5 - For L 202, L 203, and L 204

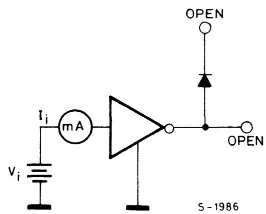


Fig. 6 - For L 201, L 202 L 203 and L 204

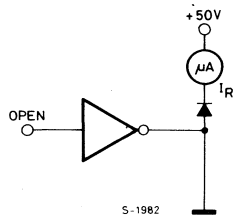


Fig. 7 - For L 202, L 203, and L 204

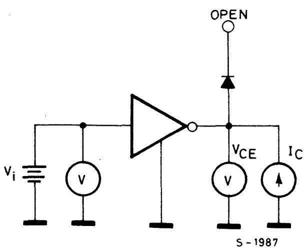
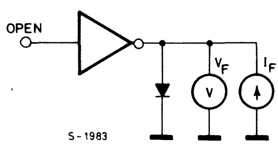
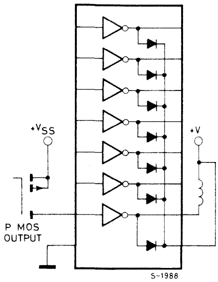


Fig. 8 - For L 201, L 202, L 203 and L 204

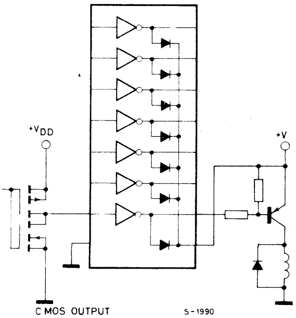


APPLICATION CIRCUITS

PMOS to load (L 202 and L 204)



Buffer for high current load (L 203 and L 204)



TTL to load (L 203)

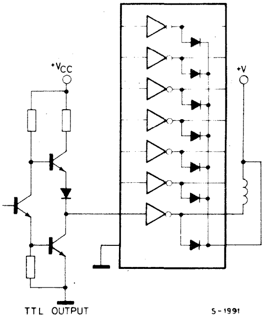


Fig. 9 - DC current gain. vs. collector current (for L 201)

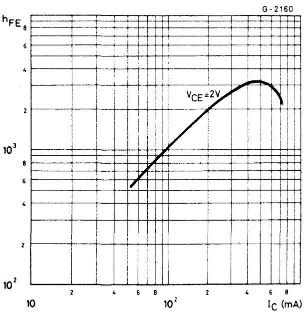


Fig. 10 - Collector current vs. collector emitter saturation voltage

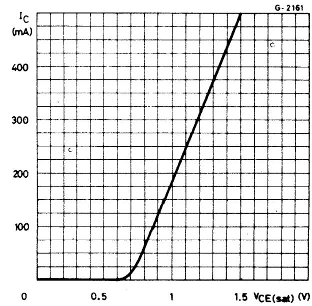


Fig. 11 - Peak collector current as a function fo duty cycle and number of outputs

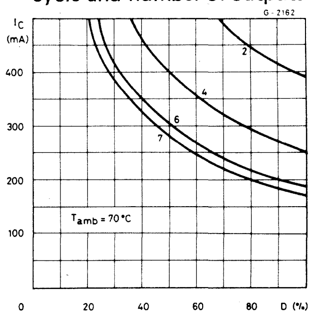


Fig. 12 - Input current vs. input voltage (for L 202 and L 204)

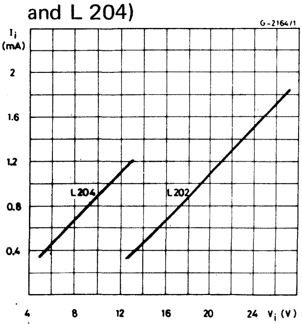


Fig. 13 - Input current vs. input voltage (L 203)

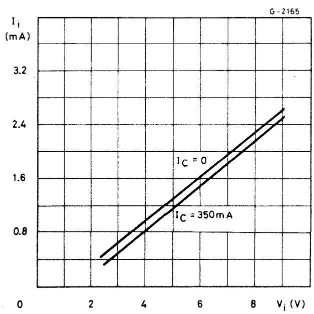
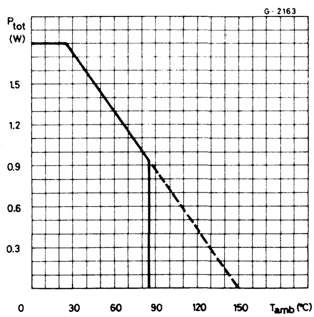


Fig. 14 - Power rating chart



LINEAR INTEGRATED CIRCUITS

L272

ADVANCE DATA

DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE RANGE
- LARGE DIFFERENTIAL MODE RANGE
- STABLE WITH UNITY GAIN
- GROUND COMPATIBLE INPUTS
- LOW SATURATION (1V/0.5A)
- THERMAL SHUTDOWN

The L272 is a monolithic integrated circuit in powerdip package, intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies.
The high gain and high output power capability provide superior performance whetever an operational amplifier/power booster combination is required.

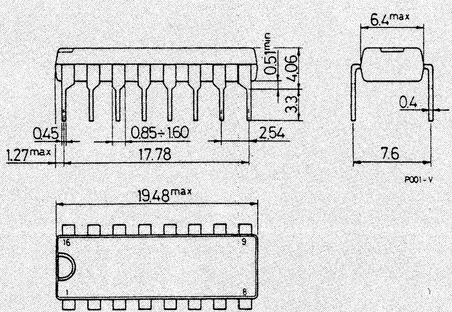
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 80°C$	1	W
	$T_{case} = 75°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

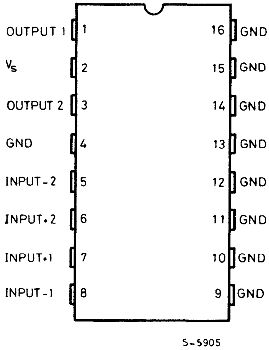
ORDERING NUMBER: L272B

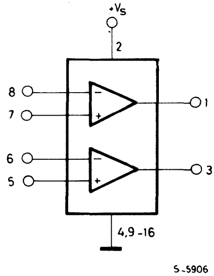
MECHANICAL DATA

Dimensions in mm

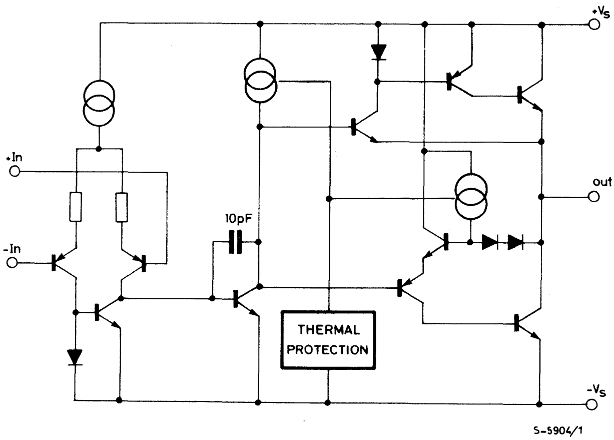


CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM



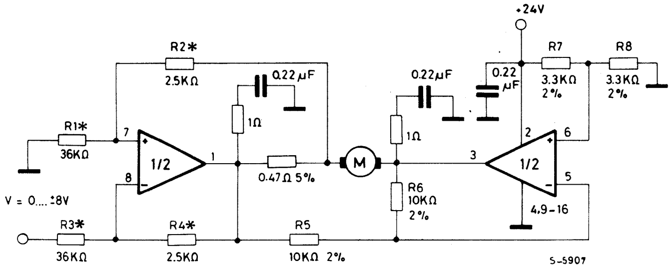
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-amb	max	70	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_d	Quiescent drain current				5.5	12	mA
I_b	Input bias current				0.5	2.5	μA
V_{os}	Input offset voltage				15		mV
I_{os}	Input offset current				50	250	nA
SR	Slew-Rate	G_V = 1			1		V/μs
B	Gain-bandwidth product				350		KHz
V_o	Output voltage swing	f = 1 kHz	I_p = 0.1A I_p = 0.5A		23 22.5		Vpp
R_i	Input resistance			500			KΩ
G_V	Voltage gain (open loop)				70		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz			5		μV
i_N	Input noise current	B = 10 to 10 000 Hz			200		pA
CMR	Common mode rejection				70		dB
SVR	Supply voltage rejection	f_{ripple} = 100 Hz	Single Supply		70		dB
			Split Supply		62		dB
T_{sd}	Thermal shutdown junction temperature				160		°C

Fig. 1 - Motor current control circuit

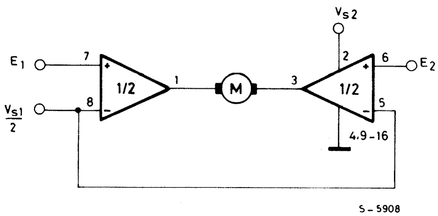


* < 1%

$I_M = 0.14 \cdot V_i$

Note: The input voltage level is compatible with L291 (5-bit D/A converter).

Fig. 2 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 3 - Bidirectional speed control of DC motors

For circuit stability ensure that $R_x > \frac{2\ R3 \cdot R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\ (V_i - \frac{V_s}{2}) + |R_o| \cdot I_M$ where $|R_o| = \frac{2\ R3 \cdot R1}{R_x}$ and I_M is the motor current;

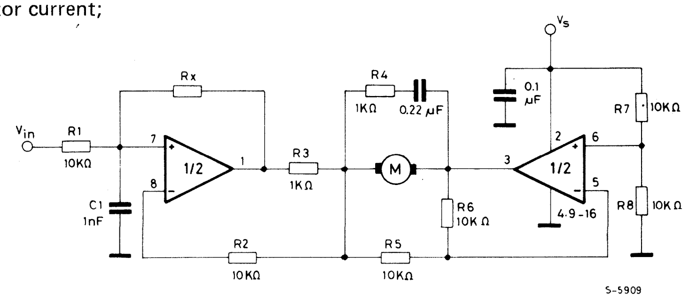
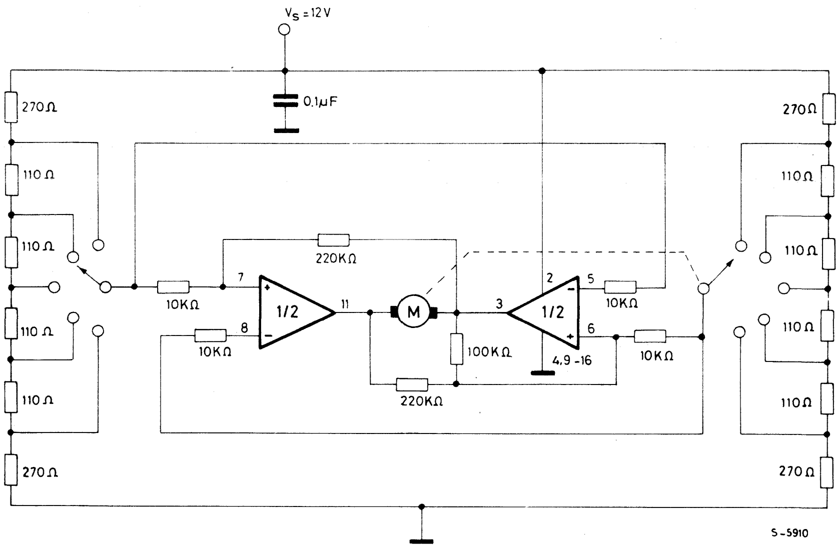


Fig. 4 - Position control for car headlights.



LINEAR INTEGRATED CIRCUITS

ADVANCE DATA

DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE RANGE
- LARGE DIFFERENTIAL MODE RANGE
- STABLE WITH UNITY GAIN
- GROUND COMPATIBLE INPUTS
- LOW SATURATION (1V/0.5A)
- THERMAL SHUTDOWN

The L272M is a monolithic integrated circuit in 8 lead minidip package, intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance whetever an operational amplifier/power booster combination is required.

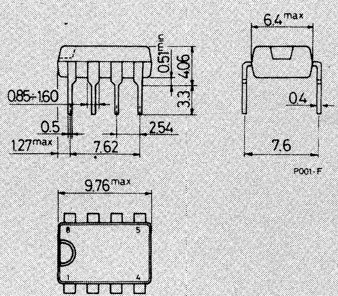
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential Input Voltage	$\pm V_s$	
I_o	DC Output Current	1	A
I_P	Peak Output Current (non repetitive)	1.5	A
P_{tot}	Power Dissipation at $T_{amb} = 50°C$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

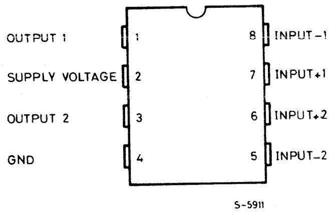
ORDERING NUMBER: L272 MB

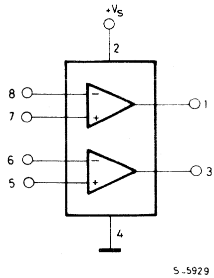
MECHANICAL DATA

Dimensions in mm

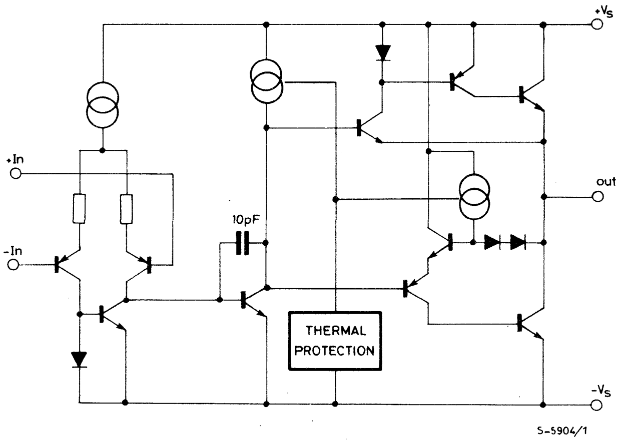


CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM



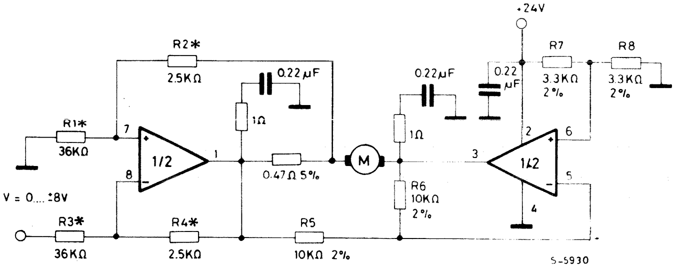
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-amb	max	100	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_d	Quiescent drain current				5.5	12	mA
I_b	Input bias current				0.5	2.5	μA
V_{os}	Input offset voltage				15		mV
I_{os}	Input offset current				50	250	nA
SR	Slew-Rate	G_v = 1			1		V/μs
B	Gain-bandwidth product				350		KHz
V_o	Output voltage swing	f = 1 kHz	I_p = 0.1A I_p = 0.5A		23 22.5		Vpp
R_i	Input resistance			500			KΩ
G_v	Voltage gain (open loop)				70		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz			5		μV
i_N	Input noise current	B = 10 to 10 000 Hz			200		pA
CMR	Common mode rejection				70		dB
SVR	Supply voltage rejection	f_{ripple} = 100 Hz	Single Supply		70		dB
		f_{ripple} = 100 Hz	Split Supply		62		dB
T_{sd}	Thermal shutdown junction temperature				160		°C

Fig. 1 - Motor current control circuit

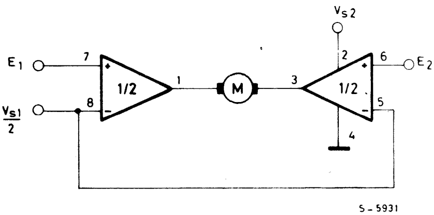


* < 1%

$$I_M = 0.14 \cdot V_i$$

Note: The input voltage level is compatible with L291 (5 - BIT D/A converter).

Fig. 2 - Bidirectional DC motor control with μP compatible inputs



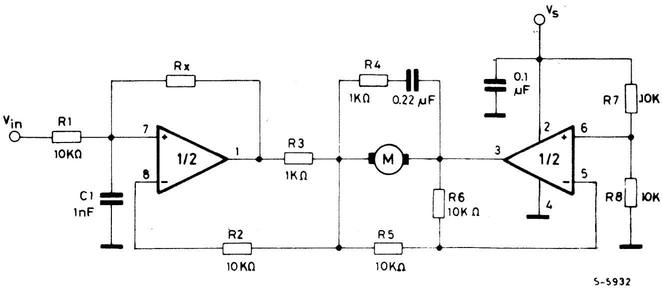
V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 3 - Bidirectional speed control of DC motors

For circuit stability ensure that $R_x > \frac{2\,R3 \cdot R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\,(V_i - \frac{V_s}{2}) + |R_o| \cdot I_M$ where $|R_o| = \frac{2\,R3 \cdot R1}{R_x}$ and I_M is the motor current.



L296

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

HIGH CURRENT SWITCHING REGULATOR

- 5.1V TO 40V OUTPUT
- 4A OUTPUT CURRENT
- DELIVERS MORE THAN 2A AT 5V WITHOUT HEATSINK
- PROGRAMMABLE CURRENT LIMITER
- SOFT START
- RESET OUTPUT
- PRECISE (± 2%) ON-CHIP REFERENCE
- VERY FEW COMPONENTS
- SWITCHING FREQUENCY TO 200 kHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- THERMAL SHUTDOWN
- REMOTE INHIBIT AND SYNC INPUT
- CONTROL CIRCUIT FOR CROWBAR SCR

The L296 is a monolithic power switching regulator delivering 4A at a voltage variable from 5.1V to 40V in step down configurations. Features of the device include programmable current limiting, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a synchronisation input for multichip configurations. The L296 is mounted in a 15-lead MULTIWATT plastic power package and requires very few external components. Efficient operation at switching frequencies up to 200 kHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

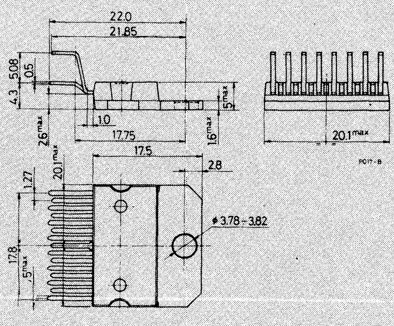
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage	50	V
$V_{i/o}$	Input/Output voltage	50	V
I_o	Output current	internally limited	
I_R	Reset output current	50	mA
V_R	Reset output voltage	50	V
V_{inh}	Inhibit voltage	15	V
P_{tot}	Power dissipation at $T_{case} < 90°C$	20	W
T_j	Junction temperature range	-25 to +150	°C
T_{stg}	Storage temperature range	-65 to +150	°C

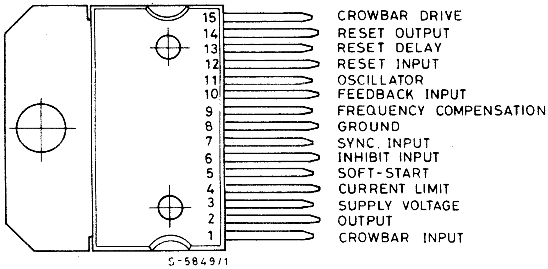
ORDERING NUMBER: L296

MECHANICAL DATA

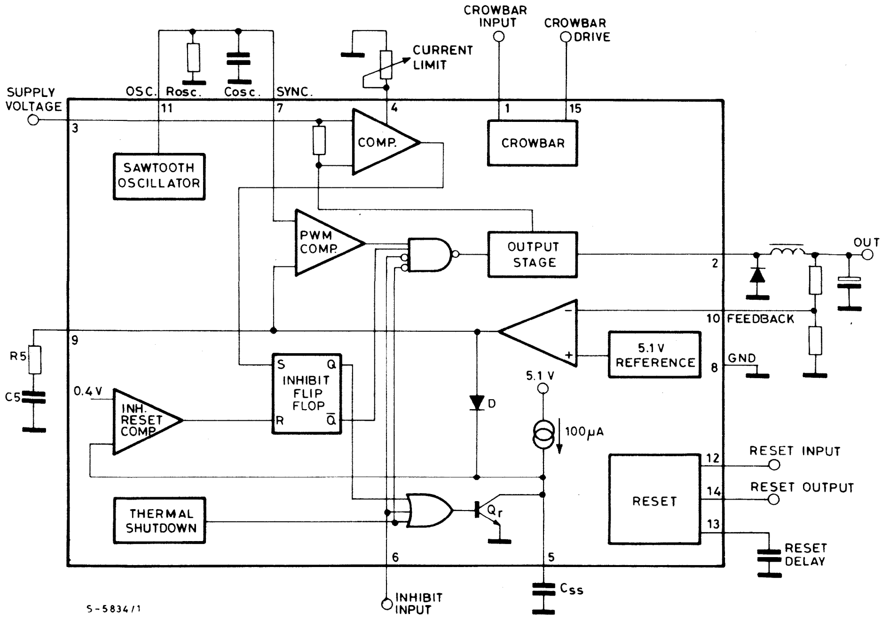
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	CROWBAR INPUT	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator output.
3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold (1.5 to 5A). If this terminal is left unconnected the threshold will be 5A.
5	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – level remote inhibit. A logic high level on this input disables the L296.
7	SYNC INPUT	Multiple L296s are synchronised by connecting the sync inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common ground terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to the sync input when the internal oscillator is used.

PIN FUNCTIONS (continued)

N°	NAME	FUNCTION
12	RESET INPUT	Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION

The L296 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.
The precision and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_s and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

CIRCUIT OPERATION (continued)

A TTL — level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches 150°C and has a hysteresis of 20°C.

Fig. 1 - Reset output waveforms

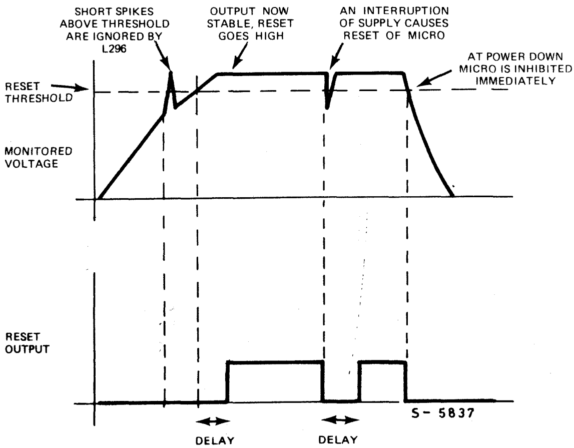


Fig. 2 - Soft start waveforms

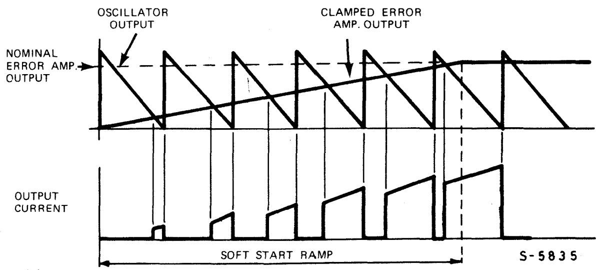
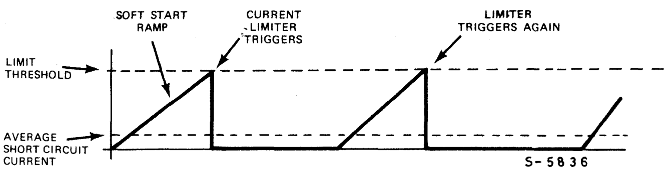


Fig. 3 - Current limiter waveforms



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C unless otherwise specified)

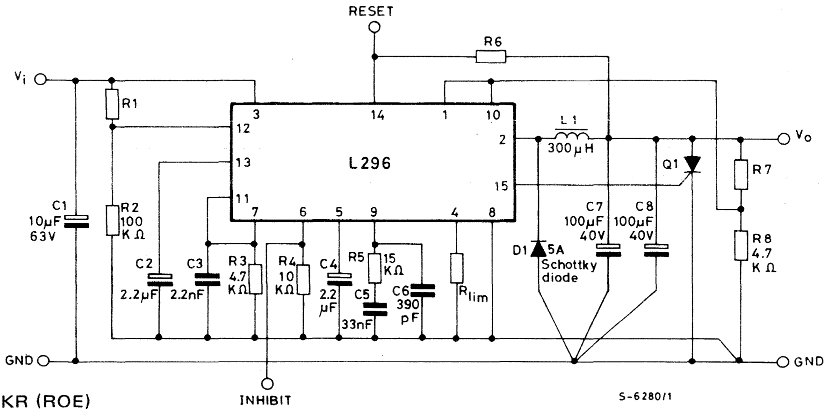
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage range		5.1		40	V
V_i	Supply voltage range		8		50	V
$I_{o\,max}$	Output current	Pin 4 open	4			A
I_{OL}	Current limit	Pin 4 open		5		A
		R_{lim} = 33 KΩ		2.5		A
V_{sat}	Output transistor saturation voltage	I_o = 4A I_o = 2A		2 1.3		V V
f_s	Switching frequency	R_{osc} = 4.7 KΩ C_{osc} = 2.2 nF		100		kHz
	Efficiency	f = 100 KHz V_i = 35V V_o = 5.1V I_o = 3A V_o = 12V		75 85		% %
V_o	Line regulation	V_i = 10 to 40V V_o = 5.1V I_o = 2A		20		mV
V_o	Load regulation	V_i = 15V V_o = 5.1V I_o = 2A to 4A I_o = 0.5A to 4A		10 15		mV mV
SVR	Supply voltage rejection	f = 100 Hz		60		dB
V_{REF}	Internally reference voltage	V_i = 8 to 50V	5	5.1	5.2	V
V_{REF}	Average temperature coeff. of reference voltage			0.2		mV/°C
t_{ss}	Stoft start time	C_s = 2.2 µF		20		ms
I_{SH}	Output average current with short circuit output			0.5		A
RESET SECTION						
V_{RTi}	Reset threshold voltage (pin 12)	V_i = 8 to 50V	V_{ref} -110mV	V_{ref} -100mV	V_{ref} -90 mV	V
V_{RTo}	Reset out low voltage (pin 14)	I_L = 16 mA			0.2	V
	Delay time (pin 13)	C_{reset} = 2.2 µF		100		ms
CROWBAR SECTION						
	Threshold voltage (pin 12)		+12%	V_{ref} +20%	+23%	
	I source — Pin 15			100		mA
	I sink — Pin 15			5		mA
	Delay time			10		µs

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INHIBIT SECTION						
V_{INHL}	Low input voltage				1.2	V
V_{INHH}	High input voltage		2.2			V
I_{INHL}	Input current with low input voltage				100	μA
I_{INHH}	Input current with high input voltage				10	μA
ERROR AMPLIFIER SECTION						
I_b	Input bias current			2		μA
G_v	Large signal open loop gain			60		dB
I_{OE}	Out sink current			200		μA
	Out source current			200		μA

Note: Measurements are performed with low duty cycle pulse signals.

Fig. 4 - Test and application circuit



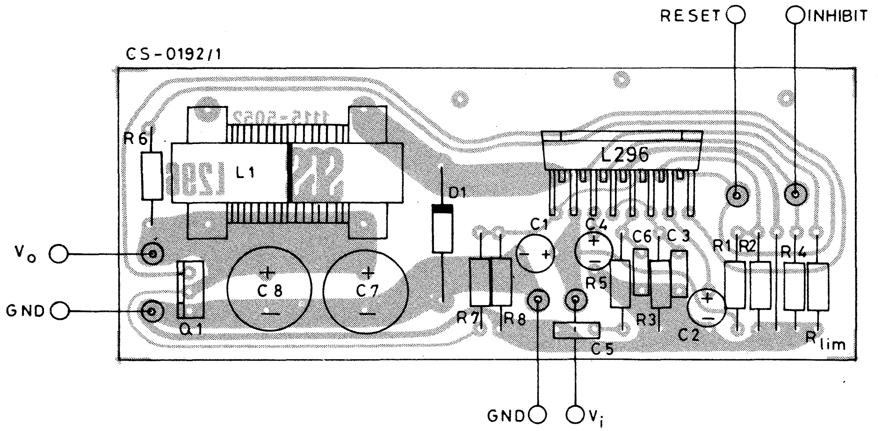
C7, C8: EKR (ROE)

SUGGESTED INDUCTOR (L1)

Core Type	No. Turns	Wire Gauge	Air Gap
Thomson GUP 20x16x7	50	0.8 mm.	0.7 mm
Siemens EC 35/17/10 (B66337 - G0500 - X127)	40	2x0.8 mm.	–
VOGT 250 µH Toroidal coil, part number 5730501800			

Resistor values for standard output voltages		
V_o	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 5 - P.C. board and component layout of the circuit of fig. 4 (1:1 scale)



SELECTION OF COMPONENT VALUES

Component	Recommended Value	Purpose	Allowed range Min.	Allowed range Max.	NOTES
R1 R2	– 100 kΩ	Set input voltage threshold for reset	–	220 kΩ	$R1/R2 = \frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be omitted and pin 12 connected to pin 10.
R3	4.7 kΩ	Sets switching frequency	1 kΩ	100 kΩ	
R_{lim}	–	Sets current limit level			If R_{lim} is omitted and pin 4 left open the current limit is 5A.
R5	15 kΩ	Frequency compensation	10 kΩ		See application note: "Designing with the L296 Power Switching Regulator"
R7 R8	– 4.7 kΩ	Divider to set output voltage	– –	– 5.1 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}}$ Omitted for 5V output.
R4	10 kΩ	Pull-down resistor		12 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R6		Collector load for reset output	$\frac{V_o}{0.05}$		Omitted if reset function not used.
C1	10 μF	Stability.	1 μF		
C2	2.2 μF	Sets reset delay	1 μF	4.7 μF	Omitted if reset function not used.
C3	2.2 nF	Sets switching frequency	1 nF	3.3 nF	
C4	2.2 μF	Soft start	1 μF	4.7 μF	Also determines average short circuit current.
C5	33 nF	Frequency compensation			See application note "Designing with the L296 Power Switching Regulator".
C6	390 pF	High frequency compensation			Not required for 5V operation.
C7, C8 L1	100 μF 300 μH	Output filter			See application note "Designing with the L296 Power Switching Regulator".
Q1		Crowbar protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.

Note: Depending on the PCB layout, component values and operating conditions, switching frequency spikes may be present on the output with an amplitude of 30 mV to 1V.
In critical applications an LC filter should be added to remove these spikes.

Fig. 6 - Efficiency vs. output current

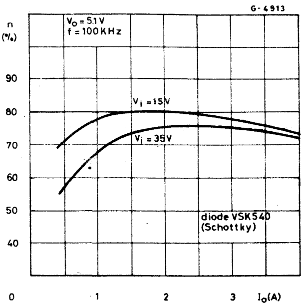


Fig. 7 - Dissipated Power vs. output current (L296 only)

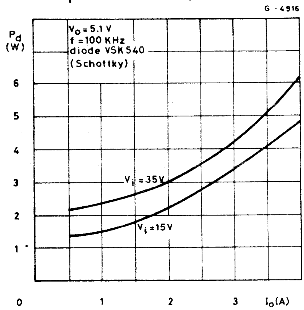


Fig. 8 - Efficiency vs. output current

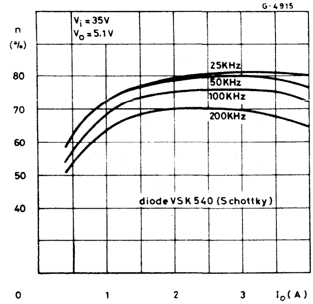


Fig. 9 - Efficiency vs. output voltage

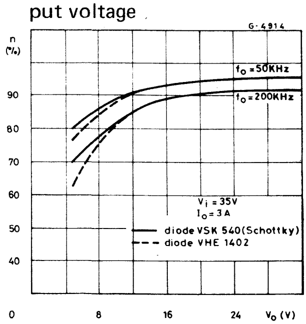


Fig. 10 - Operating frequency vs. R3 and C3

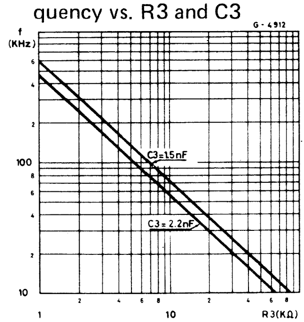


Fig. 11 - Power dissipation derating curve

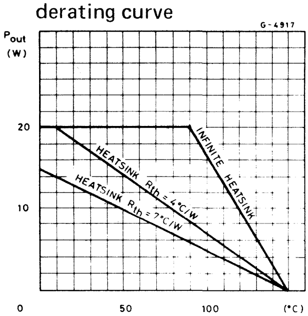


Fig. 12 - Voltage sensing for remote load

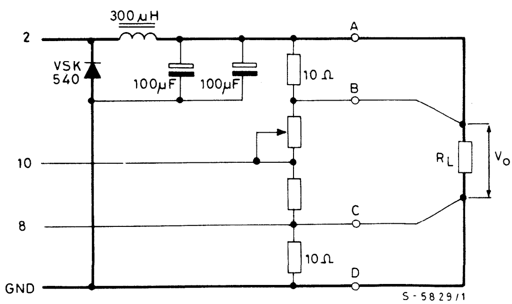
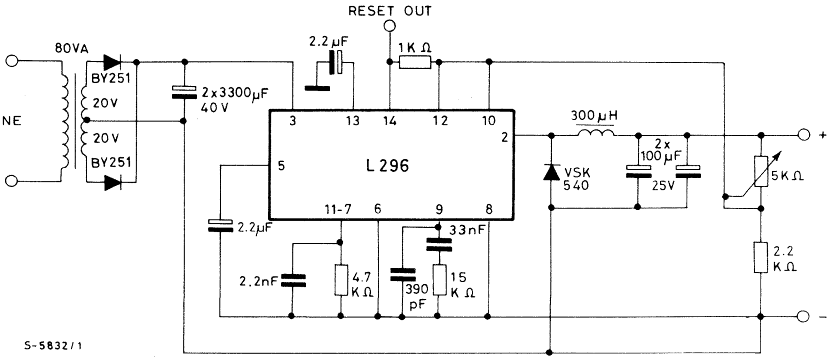
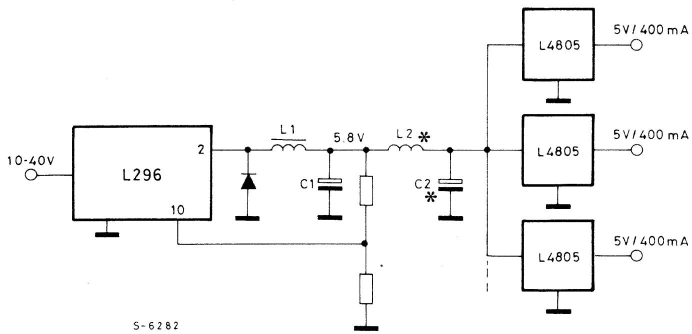


Fig. 13 - Typical application



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100 mA)
ripple ≤ 20 mV
load regulation (1A to 4A) = 10 mV (V_o = 5.1V)
line regulation (220V ± 15% and to I_o = 3A) = 15 mV (V_o = 5.1V)

Fig. 14 - Preregulator for distributed supplies



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Fig. 15 – In multiple supplies several L296s can be synchronised as shown.

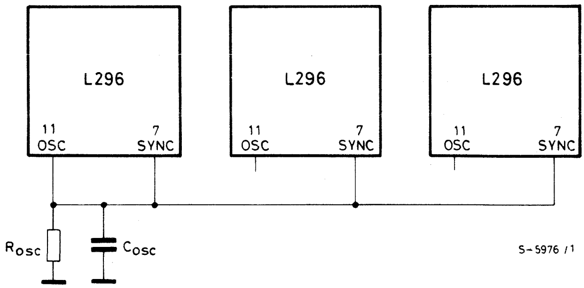
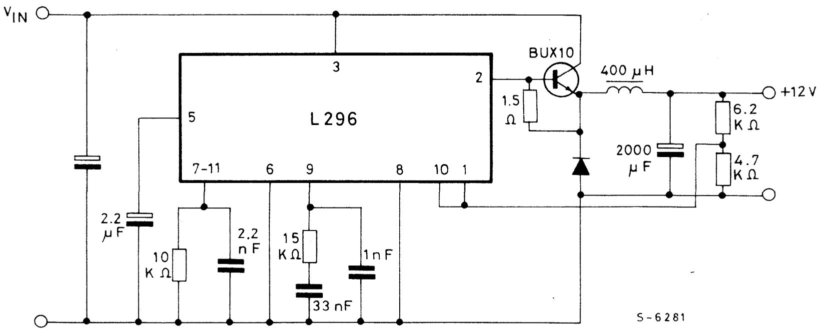


Fig. 16 – 12V/10A Power Supply



SGS

L387

LINEAR INTEGRATED CIRCUITS

ADVANCE DATA

VERY LOW DROP 5V VOLTAGE REGULATOR

- PRECISE OUTPUT VOLTAGE (5V ± 4%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500 mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)

The L387 is a very low drop voltage regulator in a PENTAWATT package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387 particularly suitable for microprocessor systems. This output provides a reset pulse when power is applied (after an externally programmable delay) and goes low when power is removed, inhibiting the microprocessor.

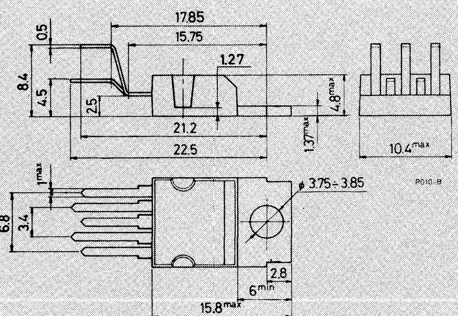
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	28	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

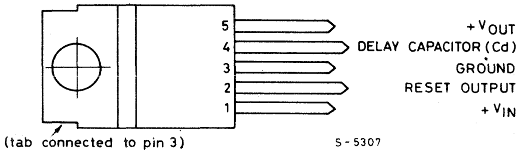
ORDERING NUMBER: L387

MECHANICAL DATA

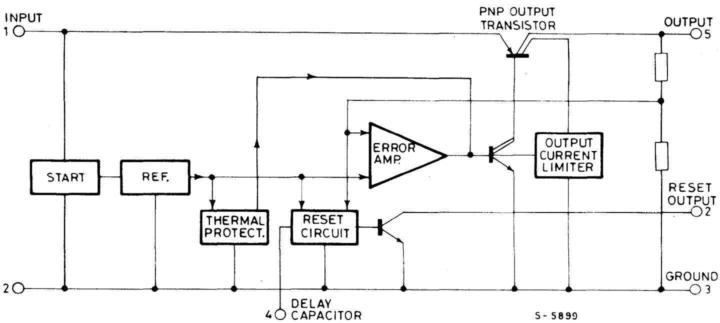
Dimensions in mm



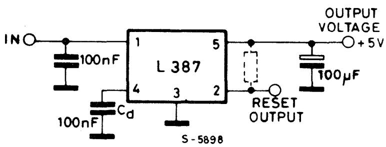
CONNECTION DIAGRAM
(top view)



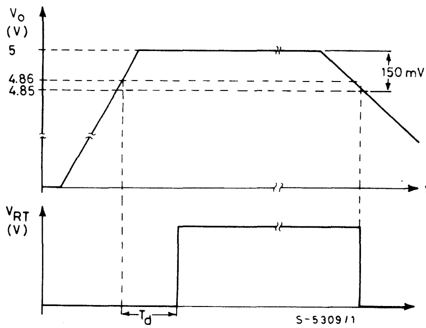
BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



TIMING DIAGRAM FOR RESET FUNCTION



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_i = 12V, T_j = 25°C, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 500 mA	4.80	5	5.20	V
V_i	Operating input voltage				26	V
ΔV_o	Line regulation	V_i = 6 to 26V I_o = 5 mA		5		mV
ΔV_o	Load regulation	I_o = 5 to 500 mA		15		mV
V_i-V_o	Dropout voltage	I_o = 500 mA		0.60	0.8	V
I_q	Quiescent current	I_o = 0 mA I_o = 150 mA I_o = 500 mA		5 20 100	— 40 300	mA
$\frac{\Delta V_o}{\Delta T}$	Temperature output voltage drift			-0.5		mV/°C
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 100 µF V_i = 12V ± 5 Vpp		60		dB
I_{sc}	Output short circuit current			0.8		A
V_R	Reset output voltage	I_R= 16 mA $V_o \leqslant$ 4.75V			0.8	V
I_R	Reset output leakage current	V_o in regulation			50	µA
t_d	Delay time for reset output	Cd = 100 nF		30		ms
V_{RT}	Reset threshold		4.75	V_o -150mV		V
V_{RTH}	Threshold hysteresis			10		mV

Fig. 1 - Dropout voltage vs. output current

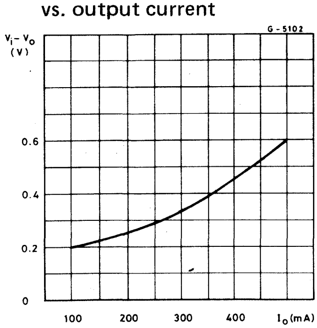


Fig. 2 - Quiescent current vs. output current

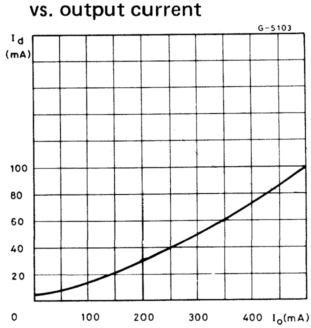
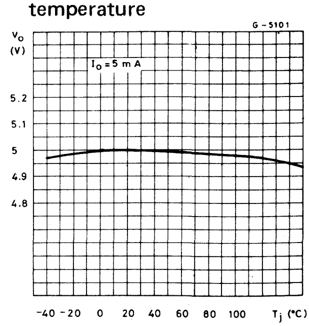


Fig. 3 - Output voltage vs. temperature



LINEAR INTEGRATED CIRCUITS

SGS **L465A**

ADVANCE DATA

HIGH EFFICIENCY POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 4A
- SUPPLY VOLTAGE TO ± 20V
- LARGE COMMON-MODE RANGE
- LARGE DIFFERENTIAL MODE RANGE
- LARGE BANDWIDTH
- LOW SATURATION
- SOA PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL PROTECTION

The L465A is a monolithic integrated circuit in PENTAWATT package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies.
The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.

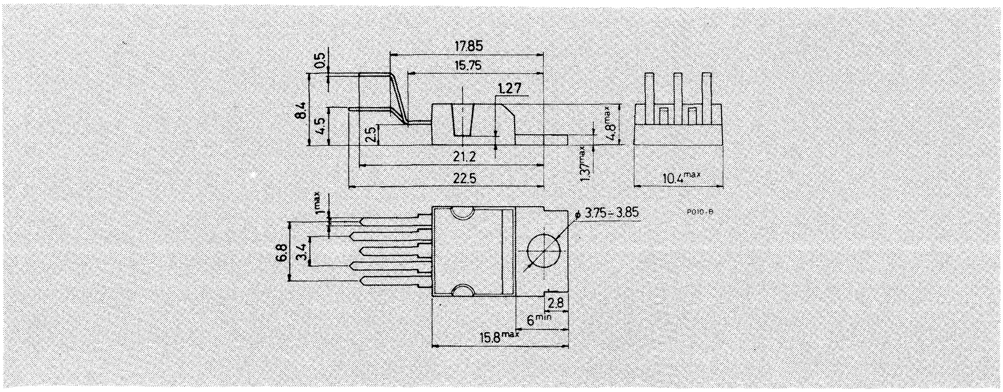
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	4	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: L465

MECHANICAL DATA

Dimensions in mm



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CONNECTION DIAGRAM
(top view)

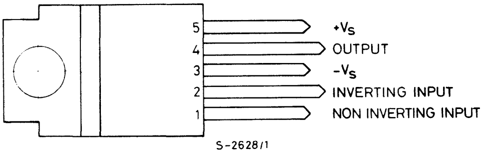


Fig. 1 - Application circuit ($G_V > 20$ dB)

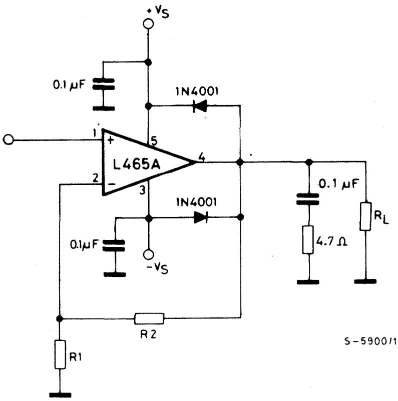
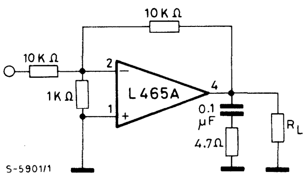


Fig. 2 - Application circuit (Unity gain)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 3		±20	V
I_d	Quiescent drain current	V_s ± 18V			45		mA
I_b	Input bias current				0.3	1	μA
V_{os}	Input offset voltage				± 2	± 20	mV
I_{os}	Input offset current					± 200	nA
SR	Slew-Rate				14		V/μs
V_o	Output voltage swing	f = 1 kHz	I_p = 0.5A I_p = 4A	26	27 25		Vpp
		f = 10 kHz	I_p = 0.5A I_p = 4A		27 24		Vpp
B_W	Power bandwidth	P_o = 1V	R_L = 4Ω		100		kHz
R_i	Input resistance (pin 1)	f = 1 KHz		100	500		KΩ
G_v	Voltage gain (open loop)				80		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz			2	6	μV
i_N	Input noise current				100		pA
CMR	Common mode rejection	R_g ≤ 10 KΩ	G_v = 30 dB		70		dB
SVR	Supply voltage rejection	R_g = 22 kΩ V_{ripple} = 0.5 V_{rms} f_{ripple} = 100 Hz	G_v = 10		60		dB
			G_v = 100		40		dB
η	Efficiency	f = 1 kHz R_L = 4Ω	I_p = 3A		66		%
T_{sd}	Thermal shutdown junction temperature				145		°C

APPLICATION INFORMATION

This circuit carries out bidirectional speed control of DC motors (fig. 3).
The motor runs in one direction or in another according to whether the input voltage is higher or lower than $V_s/2$. The output impedance of the circuit seen by the motor is $R_o = \frac{-2\,R4\;R1}{R_x}$ so by imposing that the equation $R_M = R_o$ (R_M = internal resistance of motor) is checked the maximum load regulation condition is obtained. For circuit stability it should be $R_M > |R_o|$ hence we get

$$R_X > \frac{2\,R4 \cdot R1}{R_M}$$

The voltage available at the terminals of the motor is

$$V_M = 2\left(V_{in} - \frac{V_s}{2}\right) + |R_o| \cdot I$$

Fig. 3 - Bidirectional speed control of DC motors

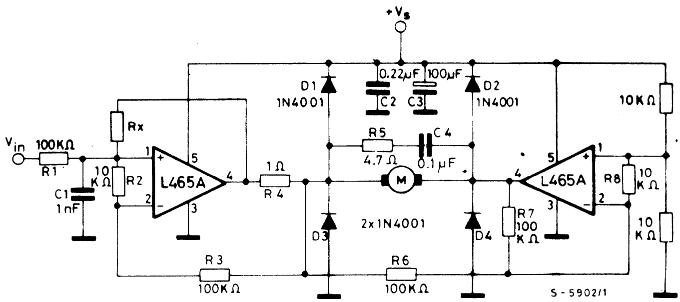
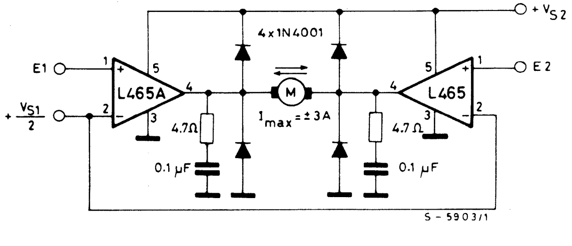


Fig. 4 - Bidirectional DC motor control with TTL/C-MOS/µP compatible inputs



V_{S1} = logic supply voltage Must be $V_{S2} \geqslant V_{S1}$ E1, E2 = logic inputs

LINEAR INTEGRATED CIRCUITS

SGS **L487**

PRELIMINARY DATA

VERY LOW DROP 5V VOLTAGE REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5V ± 4%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500 mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- + 80/-80V LOAD DUMP PROTECTION
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

The L487 is a monolithic integrated circuit in PENTAWATT package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L487 can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems: a pulse is available (after an externally programmable delay) to reset the microprocessor at power-on phase; at power-off, this pulse becomes low inhibiting the microprocessor.

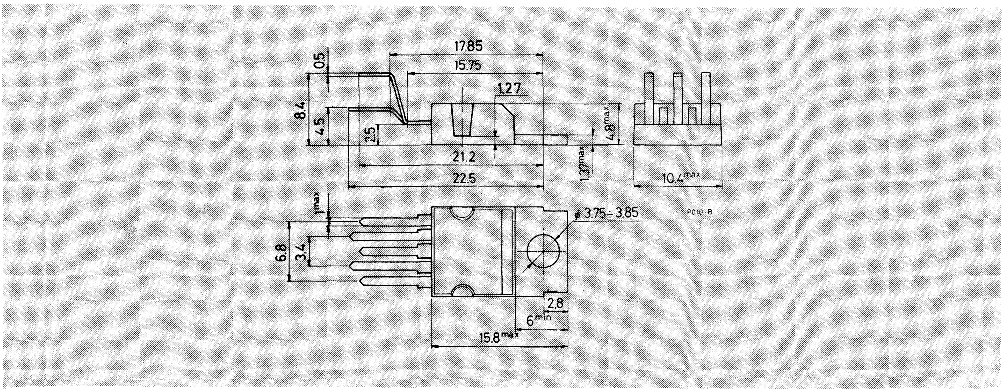
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	35	V
V_i	Reverse input voltage	-18	V
	Positive transient peak voltage (t = 300 ms)	80	V
	Negative transient peak voltage (t = 100 ms)	-80	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

ORDERING NUMBER: L487

MECHANICAL DATA

Dimensions in mm



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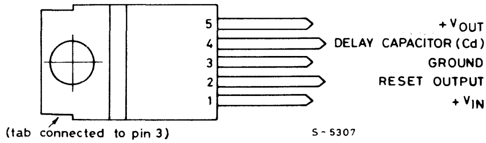
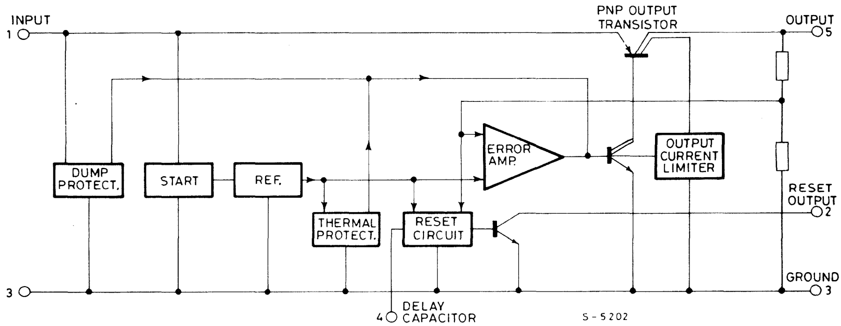
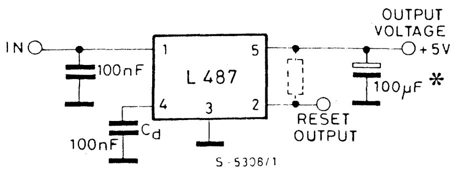
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM

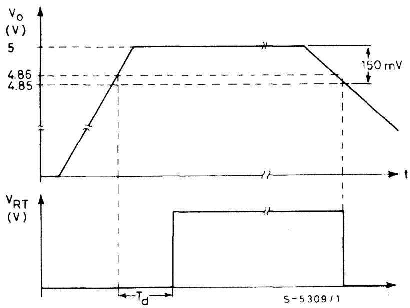


TEST AND APPLICATION CIRCUIT



* Min. 20 µF

TIMING DIAGRAM FOR RESET FUNCTION



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_i = 14.4V, T_{amb} = 25°C, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 500 mA	4.80	5	5.20	V
V_i	Operating input voltage	(*) See note			28	V
ΔV_o	Line regulation	V_i = 6 to 26V I_o = 5 mA		5		mV
ΔV_o	Load regulation	I_o = 5 to 500 mA		15		mV
V_i-V_o	Dropout voltage	I_o = 500 mA		0.6	0.8	V
I_q	Quiescent current	I_o = 0 mA I_o = 150 mA I_o = 500 mA		6 20 130	40	mA
$\frac{\Delta V_o}{\Delta T}$	Temperature output voltage drift			-0.5		mV/°C
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 100 µF V_i = 12V ± 5 Vpp		55		dB
I_{sc}	Output short circuit current			0.8		A
V_R	Reset output voltage	I_R = 16 mA $V_o \leq$ 4.75V			0.8	V
I_R	Reset output leakage current	V_o in regulation			50	µA
t_d	Delay time for reset output	Cd = 100 nF		30		ms
V_{RT}	Reset threshold		4.75	V_o-0.15		V
V_{RTH}	Threshold hysteresis			10		mV

(*) For a DC input voltage 28 < V_i < 35V the device is not operating.

Fig. 1 - Dropout voltage vs. output current

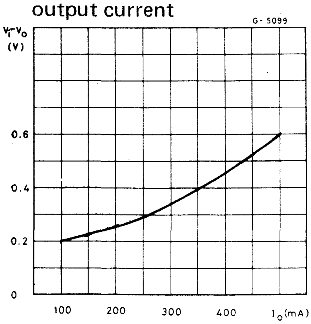


Fig. 2 - Quiescent current vs. output current

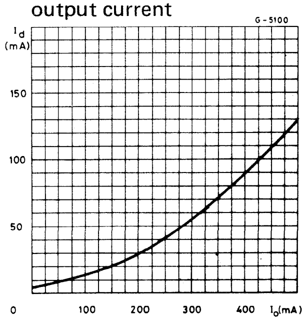
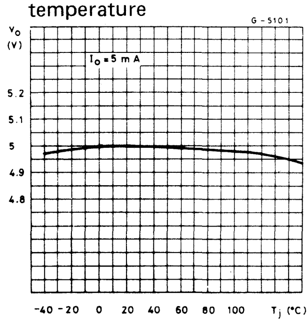


Fig. 3 - Output voltage vs. temperature



L601 L602
L603 L604

LINEAR INTEGRATED CIRCUITS

DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400 mA PER DRIVER (500 mA peak)
- OUTPUT VOLTAGE 90V ($V_{CE(sus)}$ = 70V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can withstand peak currents of 500 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

L601	General purpose, DTL, TTL, PMOS, CMOS
L602	14-25V PMOS
L603	5V TTL, CMOS
L604	6 - 15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.
The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.

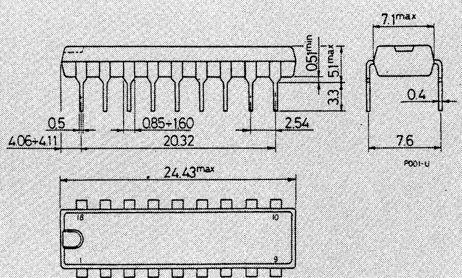
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector emitter voltage (input open)	90	V
I_C	Collector current	0.4	A
I_C	Collector peak current	0.5	A
V_i	Input voltage (for L602, L603 and L604)	30	V
I_i	Input current (for L601 only)	25	mA
P_{tot}	Total power dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

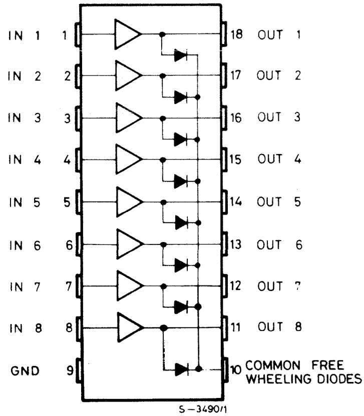
ORDERING NUMBERS: L601B, L602B, L603B, L604B

MECHANICAL DATA

Dimensions in mm

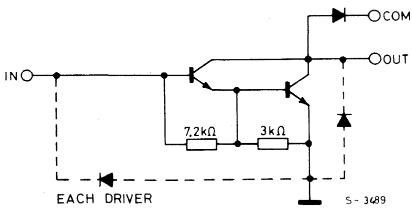


CONNECTION DIAGRAM
(top view)

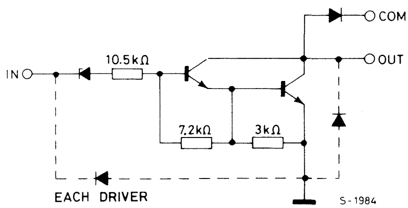


SCHEMATIC DIAGRAMS

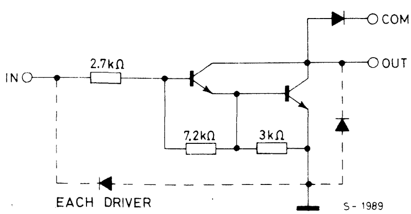
L601



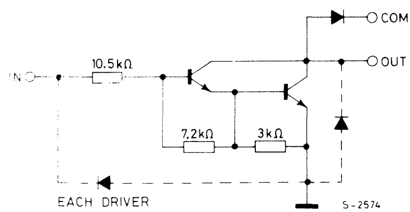
L602



L603



L604



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE}= 90V			10	μA
$V_{CE(sat)}$	Collector emitter saturation voltage	I_C= 300 mA I_B= 500 μA I_C= 200 mA I_B= 350 μA I_C= 100 mA I_B= 250 μA			2 1.7 1.2	V V V
h_{FE}	DC forward current gain (L601 only)	V_{CE}= 3V I_C= 300 mA	1000			–
V_i	Minimum input voltage (ON condition)	V_{CE}= 3V I_C= 300 mA for L602 for L603 for L604			 11.5 2.5 2.5	 V V V
V_i	Maximum input voltage (OFF condition)	V_{CE}= 90V I_C= 25 μA for L601 for L602 for L603 for L604	 0.55 7 0.75 1			 V V V V
I_R	Clamp diode reverse current	V_R= 90V			50	μA
V_F	Clamp diode forward voltage	I_F= 300 mA		2	2.4	V
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o		0.4		μs
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o		0.4		μs

LINEAR INTEGRATED CIRCUITS

SGS

L2605
L2685
L2610

PRELIMINARY DATA

VOLTAGE REGULATORS FOR AUTOMOTIVE AND INDUSTRIAL APPLICATIONS

- OUTPUT VOLTAGE OF 5, 8.5 AND 10V
- OUTPUT CURRENT UP TO 500 mA
- NO EXTERNAL COMPONENTS
- LOW DROP-OUT VOLTAGE
- LOAD DUMP VOLTAGE SURGE PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION
- CURRENT LIMITING
- THERMAL SHUTDOWN

The L2600 series of three terminal positive regulators is specially designed to stabilize power supplies for car instrumentation in vehicles with 12V battery. They can supply an output current up to 500 mA.

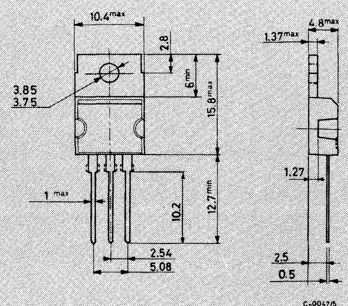
ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	35	V
V_i	DC input reverse voltage	-28	V
V_d	Positive transient peak voltage (t = 40 ms, duty cycle = 1%)	+ 100	V
V_d	Negative transient peak voltage (t = 30 ms, duty cycle = 1%)	- 100	V
T_{op}	Operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-65 to 150	°C
P_{tot}	Power dissipation	Internally limited	

ORDERING NUMBERS: L2605V (V_o= 5V)
L2685V (V_o= 8.5V)
L2610V (V_o= 10V)

MECHANICAL DATA

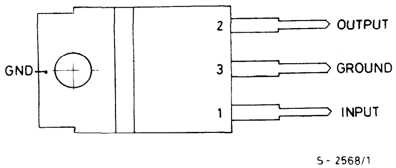
Dimensions in mm

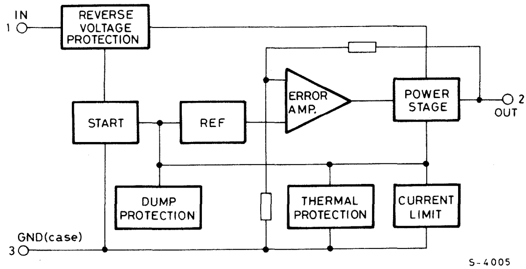


3/83

L2605
L2685
L2610

CONNECTION AND BLOCK DIAGRAMS
(top view)





THERMAL DATA

$R_{th\,j\text{-}case}$	Thermal resistance junction-case	max.	4 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 500 mA	V_i = 12 to 16V (L2605) V_i = 12 to 16V (L2685) V_i = 12 to 16V (L2610)	4.8 8.15 9.55	5 8.5 10	5.2 8.85 10.45	V
V_i	Operating input voltage	see note (°)				28	V
ΔV_o	Line regulation	I_o = 50 mA	V_i = 12 to 16V		2		mV
$\frac{\Delta V_o}{V_o}$	Load regulation	V_i = 14V	I_o = 50 to 500 mA		0.3		%
$\Delta V_{i\text{-}o}$	Dropout voltage	I_o = 500 mA				1.9	V
I_d	Quiescent current	I_o = 500 mA			15		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 50mA V_i = 14V T_{amb} = −12 to 80° C			−1		mV/°C
I_{sc}	Output short circuit current	V_i = 14V			900		mA
SVR	Supply voltage rejection	V_i = 16V ΔV_i = 2V f = 100Hz I_o = 500mA			60		dB
R_o	Output resistance	I_o = 500mA			0.05		Ω
e_N	Output noise voltage	BW = 100Hz to 10KHz			20		μV

(°) Note: For a DC input voltage 28V < V_i < 35V the device is not operating

LINEAR INTEGRATED CIRCUITS

L4705
L4785
L4710

PRELIMINARY DATA

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.6V
- 500 mA OUTPUT CURRENT
- 80V LOAD DUMP PROTECTION
- -80V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- OUTPUT CURRENT LIMITING
- THERMAL SHUTDOWN

L4700 series voltage regulators feature a very low voltage drop, an output current of 500 mA and protection against load dump transients of ± 80V. Available in 5V, 8.5V and 10V (±4%) versions, these regulators also include reverse polarity protection, overvoltage protection, output current limiting and a thermal shutdown circuit.
L4700 series regulators are specially designed for automotive and industrial applications where the electrical environment is very demanding and low voltage drop is required. For example, the L4705 can be used in 5V automotive applications, continuing to function even when the battery voltage falls to 6V, a common event during starting. Moreover, the L4705 is fully protected against the transients, overvoltages and polarity reversal encountered on the battery rail.

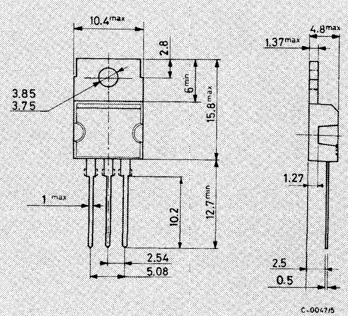
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	35	V
V_i	Reverse input voltage	-18	V
V_t	Positive transient peak voltage (t = 300 ms)	+ 80	V
V_t	Negative transient peak voltage (t = 100 ms)	-80	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

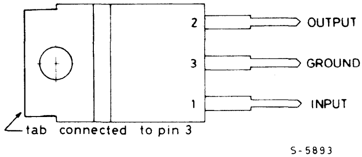
ORDERING NUMBER: L4705CV (5V), L4785CV (8.5V), L4710CV (10V)

MECHANICAL DATA

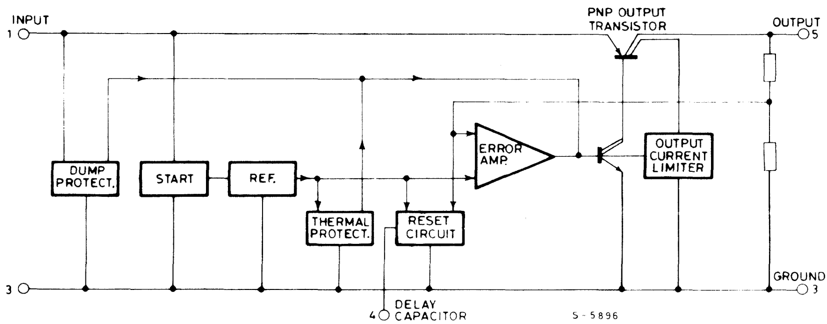
Dimensions in mm



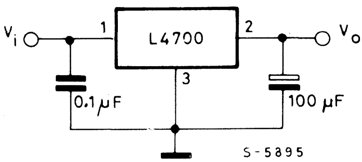
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS ($V_i = 14.4V$, $T_j = 25°C$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 500 mA	4.80	5	5.20	V
			8.16	8.5	8.84	V
			9.6	10	10.4	V
V_i	Operating input voltage	(*) see note			28	V
$\Delta V_o/V_o$	Line regulation	V_i = 11 to 26V I_o = 5 mA		1		mV/V
$\Delta V_o/V_o$	Load regulation	I_o = 5 to 500 mA		3		mV/V
$V_i - V_o$	Dropout voltage	I_o = 500 mA		0.6	0.9	V
I_q	Quiescent current	I_o = 0 mA		6		mA
		I_o = 150 mA		20	40	mA
		I_o = 500 mA		130		mA
$\frac{\Delta V_o}{\Delta T \cdot V_o}$	Temperature output voltage drift			0.1		$\frac{mV}{°C \cdot V}$
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 100 μF $V_i=V_o+3V+2V_{pp}$		55		dB
I_{sc}	Output short circuit current			800		mA

(*) For a DC input voltage 28V < V_i < 35V the device is not operating.

Fig. 1 - Dropout voltage vs. output current

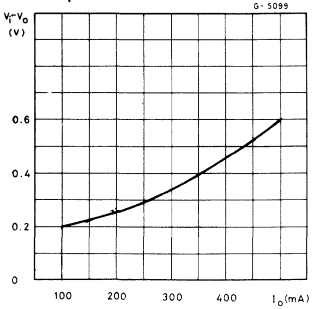


Fig. 2 - Quiescent current vs. output current

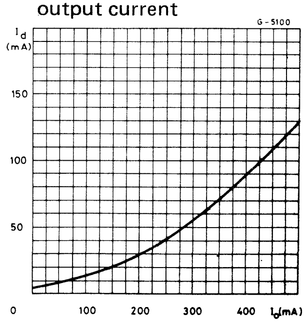
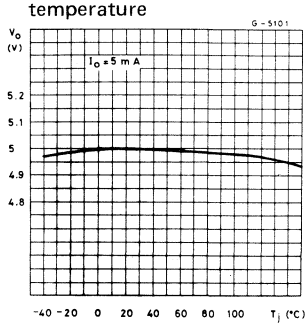


Fig. 3 - Output voltage vs. temperature



SGS

L4805
L4885
L4810

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.4V
- 400 mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- 60V LOAD DUMP PROTECTION
- -60V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

L4800 series devices are voltage regulators with a very low voltage drop (typically 0.4V at full rated current), output current up to 400 mA, low quiescent current and comprehensive on-chip protection. These devices are protected against load dump transients of ± 60V, input overvoltage, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V and 10V versions (all ± 4%), these regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.
In automotive applications the L4805 is ideal for 5V logic supplies because it functions with battery voltages as low as 5.5V. In battery backup and standby applications the low consumption of these devices extends battery life.

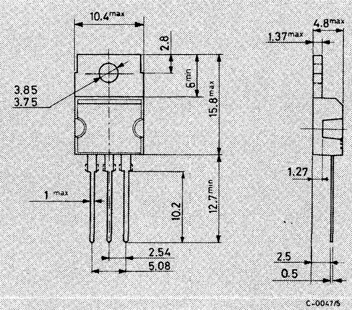
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	26	V
V_i	Reverse input voltage	-18	V
V_t	Positive transient peak voltage (t = 300 ms)	+60	V
V_t	Negative transient peak voltage (t = 100 ms)	-60	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

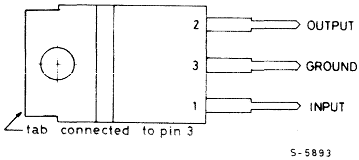
ORDERING NUMBER: L4805CV (5V), L4885CV (8.5V), L4810CV (10V)

MECHANICAL DATA

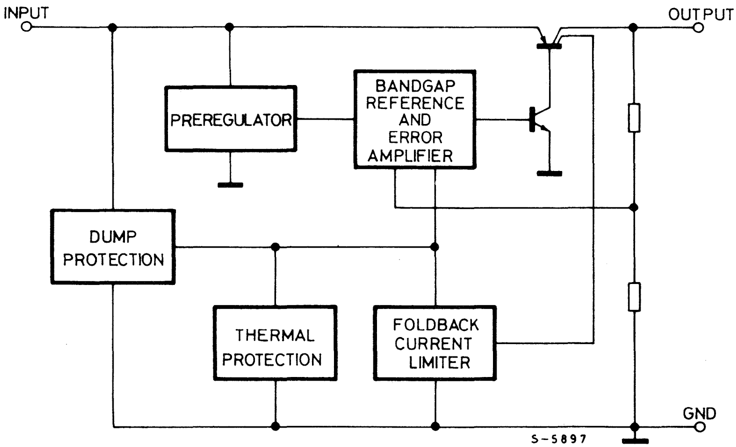
Dimensions in mm



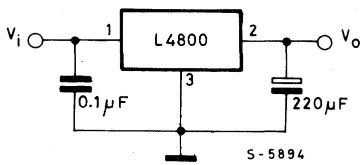
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

L4805
L4885
L4810

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, T_j = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 400 mA	4.80	5	5.20	V
			8.16	8.5	8.84	V
			9.6	10	10.4	V
V_i	Operating input voltage				26	V
$\Delta V_o/V_o$	Line regulation	V_i = 11 to 26V I_o = 5 mA		1	10	mV/V
$\Delta V_o/V_o$	Load regulation	I_o = 5 to 400 mA		3	15	mV/V
V_i-V_o	Dropout voltage	I_o = 400 mA		0.4	0.7	V
		I_o = 150 mA		0.2	0.4	V
I_q	Quiescent current	I_o = 0 mA		0.8	3	mA
		I_o = 150 mA		16	45	mA
		I_o = 400 mA		80	100	mA
$\frac{\Delta V_o}{\Delta T \cdot V_o}$	Temperature output voltage drift			0.1		$\frac{mV}{°C \cdot V}$
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 100 μF V_i=V_o+3V+2V_{pp}		60		dB
I_o	Max output current			750		mA
I_{sc}	Output short circuit current (fold back condition)			220		mA

Fig. 1 - Dropout voltage vs. output current

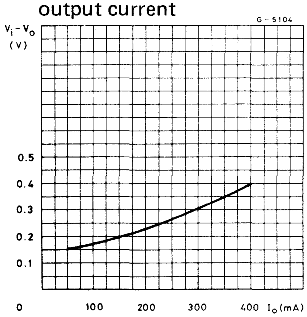


Fig. 2 - Quiescent current vs. output current

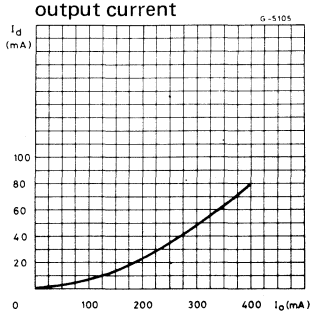


Fig. 3 - Output voltage vs. temperature

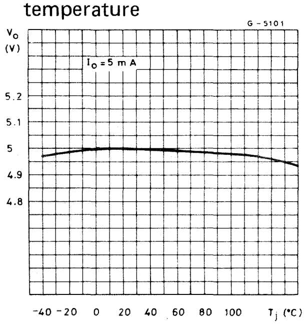


Fig. 4 - Foldback current limiting (L4805)

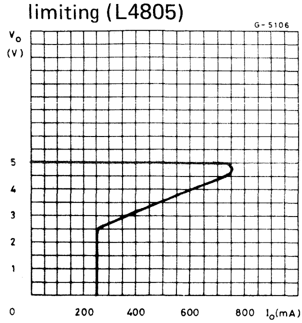
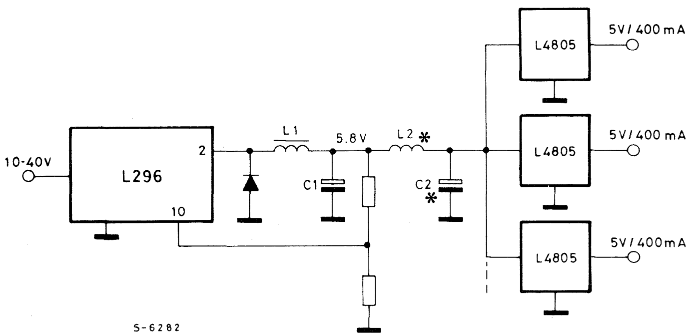


Fig. 5 - Preregulator for distributed supplies



SGS

L7800 Series

LINEAR INTEGRATED CIRCUITS

POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

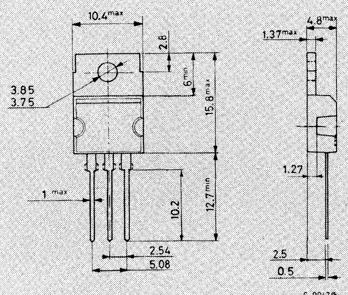
The L7800 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

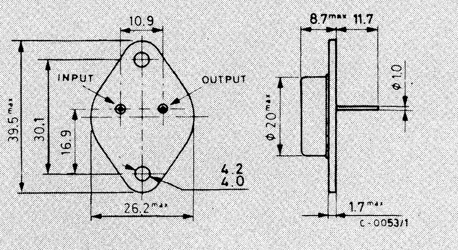
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{op}	Operating junction temperature (for **L7800**)	-55 to +150	°C
	(for **L7800C**)	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

MECHANICAL DATA

Dimensions in mm



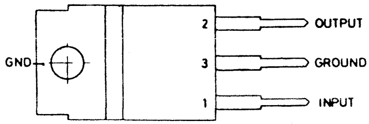
TO-220

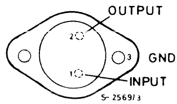


TO-3

CONNECTION DIAGRAMS AND ORDERING NUMBERS

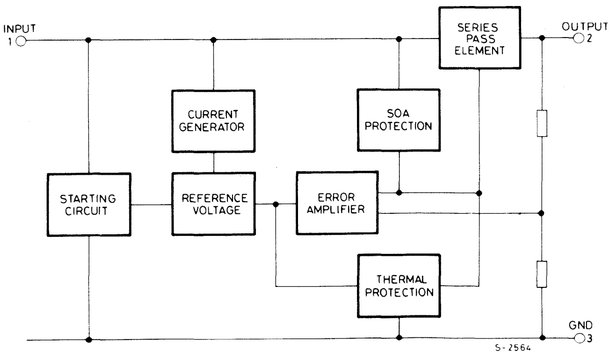
(top views)





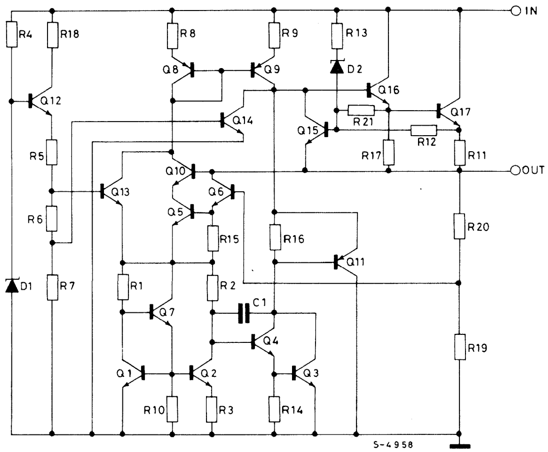
Type	TO-220	TO-3	Output voltage
L 7805	–	L 7805T	5V
L 7805C	L 7805CV	L 7805 CT	5V
L 7806	–	L 7806T	6V
L 7806C	L 7806 CV	L 7806CT	6V
L 7808	–	L 7808T	8V
L 7808C	L 7808 CV	L 7808CT	8V
L 7812	–	L 7812T	12V
L 7812C	L 7812CV	L 7812CT	12V
L 7815	–	L 7815T	15V
L 7815C	L 7815CV	L 7815CT	15V
L 7818	–	L 7818T	18V
L 7818C	L 7818CV	L 7818CT	18V
L 7820	–	L 7820T	20V
L 7820C	L 7820CV	L 7820CT	20V
L 7824	–	L 7824T	24V
L 7824C	L 7824CV	L 7824CT	24V

BLOCK DIAGRAM



L7800 Series

SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

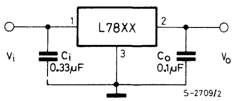


Fig. 2 - Load regulation

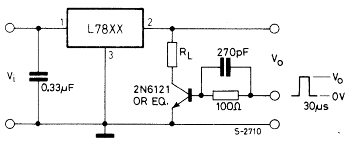
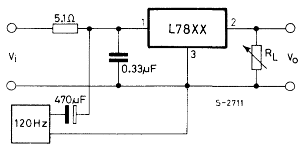


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L 7800 (Refer to the test circuits, T_j= -55 to 150°C, I_o = 500 mA, C_i = 0.33 μF, C_o= 0.1 μF unless otherwise specified)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o= 5 mA to 1A $P_o \leq$ 15W	4.65	5	5.35	5.65	6	6.35	7.6	8	8.4	11.4	12	12.6	V
				(V_i= 8 to 20V)			(V_i= 9 to 21V)			(V_i= 11.5 to 23V)			(V_i= 15.5 to 27V)		
ΔV_o	Line regulation	T_j= 25°C			50			60			80			120	mV
				(V_i= 7 to 25V)			(V_i= 8 to 25V)			(V_i= 10.5 to 25V)			(V_i= 14.5 to 30V)		
					25			30			40			60	mV
				(V_i= 8 to 12V)			(V_i= 9 to 13V)			(V_i= 11 to 17V)			(V_i= 16 to 22V)		
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			100			100			100			120	mV
		T_j= 25°C I_o= 250 to 750 mA			25			30			40			60	mV
I_d	Quiescent current	T_j= 25°C			6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					0.8			0.8			0.8			0.8	mA
				(V_i= 8 to 25V)			(V_i= 9 to 25V)			(V_i= 11.5 to 25V)			(V_i= 15 to 30V)		
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		0.6			0.7			1			1.5		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz T_j= 25°C			40			40			40			40	$\frac{\mu V}{V_o}$
SVR	Supply voltage rejection	f = 120 Hz	68			65			62			61			dB
				(V_i= 8 to 18V)			(V_i= 9 to 19V)			(V_i= 11.5 to 21.5V)			(V_i= 15 to 25V)		
V_d	Dropout voltage	I_o= 1A T_j= 25°C		2	2.5		2	2.5		2	2.5		2	2.5	V
R_o	Output resistance	f = 1 KHz		17			19			16			18		mΩ
I_{sc}	Short circuit current	V_i= 35V T_j= 25°C		0.75	1.2		0.75	1.2		0.75	1.2		0.75	1.2	A
I_{scp}	Short circ. peak current	T_j= 25°C	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS L 7800 (continued)

OUTPUT VOLTAGE		15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)		23			26			28			33			
Parameter	Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o Output voltage	T_j = 25°C	14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
	I_o = 5 mA to 1A $P_o \leq$ 15W	14.25 (V_i = 18.5 to 30V)	15	15.75	17.1 (V_i = 22 to 33V)	18	18.9	19 (V_i = 24 to 35V)	20	21	22.8 (V_i = 28 to 38V)	24	25.2	V
ΔV_o Line regulation	T_j = 25°C	(V_i = 17.5 to 30V)		150	(V_i = 21 to 33V)		180	(V_i = 22.5 to 35V)		200	(V_i = 27 to 38V)		240	mV
		(V_j = 20 to 26V)		75	(V_i = 24 to 30V)		90	(V_i = 26 to 32V)		100	(V_i = 30 to 36V)		120	mV
ΔV_o Load regulation	T_j = 25°C I_o = 5 mA to 1.5A			150			180			200			240	mV
	T_j = 25°C I_o = 250 to 750 mA			75			90			100			120	mV
I_d Quiescent current	T_j = 25°C			6			6			6			6	mA
ΔI_d Quiescent current change	I_o = 5 mA to 1A			0.5			0.5			0.5			0.5	mA
		(V_i = 18.5 to 30V)		0.8	(V_i = 22 to 33V)		0.8	(V_i = 24 to 35V)		0.8	(V_i = 28 to 38V)		0.8	mA
$\frac{\Delta V_o}{\Delta T}$ Output voltage drift	I_o = 5 mA		1.8			2.3			2.5			3		mV/°C
e_N output noise voltage	B = 10Hz to 100KHz T_j = 25°C		40			40			40			40		$\frac{\mu V}{V_o}$
SVR Supply voltage rejection	f = 120 Hz	60 (V_i = 18.5 to 28.5V)			59 (V_i = 22 to 32V)			58 (V_i = 24 to 35V)			56 (V_i = 28 to 38V)			dB
V_d Dropout voltage	I_o = 1A T_j = 25°C		2	2.5		2	2.5		2	2.5		2	2.5	V
R_o Output resistance	f = 1 KHz		19			22			24			28		mΩ
I_{sc} Short circuit current	V_i = 35V T_j = 25°C		0.75	1.2		0.75	1.2		0.75	1.2		0.75	1.2	A
I_{scp} Short circ. peak current	T_j = 25°C	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS L 7800C (Refer to the test circuits, T_j = 0 to 125°C, I_o = 500 mA, C_i = 0.33 μF, C_o = 0.1 μF unless otherwise specified)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o = 5 mA to 1A $P_o \leqslant$ 15W	4.75	5	5.25	5.7	6	6.3	7.6	8	8.4	11.4	12	12.6	V
				(V_i = 7 to 20V)			(V_i = 8 to 21V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 27V)		
ΔV_o	Line regulation	T_j = 25°C		3	100			120			160			240	mV
				(V_i = 7 to 25V)			(V_i = 8 to 25V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 30V)		
				1	50			60			80			120	mV
				(V_i = 8 to 12V)			(V_i = 9 to 13V)			(V_i = 11 to 17V)			(V_i = 16 to 22V)		
ΔV_o	Load regulation	T_j = 25°C I_o = 5 mA to 1.5A			100			120			160			240	mV
		T_j = 25°C I_o = 250 to 750 mA			50			60			80			120	mV
I_d	Quiescent current	T_j = 25°C			8			8			8			8	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3			1.3			1			1	mA
				(V_i = 7 to 25V)			(V_i = 8 to 25V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 30V)		
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 5 mA		-1.1			-0.8			-0.8			-1		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz T_j = 25°C		40			45			52			75		μV
SVR	Supply voltage rejection	f = 120 Hz	62			59			56			55			dB
				(V_i = 8 to 18V)			(V_i = 9 to 19V)			(V_i = 11.5 to 21.5V)			(V_i = 15 to 25V)		
V_d	Dropout voltage	I_o = 1A		2			2			2			2		V
R_o	Output resistance	f = 1 KHz		17			19			16			18		mΩ
I_{sc}	Short circuit current	V_i = 35V T_j = 25°C		750			550			450			350		mA
I_{scp}	Short circ. peak current	T_j = 25°C		2.2			2.2			2.2			2.2		A

ELECTRICAL CHARACTERISTICS L 7800C (continued)

OUTPUT VOLTAGE		15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)		23			26			28			33			
Parameter	Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o Output voltage	T_j= 25°C	14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
	I_o= 5 mA to 1A, $P_o \leqslant$ 15W	14.25	15	15.75	17.1	18	18.9	19	20	21	22.8	24	25.2	V
		(V_i= 17.5 to 30V)			(V_i= 21 to 33V)			(V_i= 23 to 35V)			(V_i= 27 to 38V)			
ΔV_o Line regulation	T_j= 25°C			300 (V_i= 17.5 to 30V)			360 (V_i= 21 to 33V)			400 (V_i= 22.5 to 35V)			480 (V_i= 27 to 38V)	mV
				150 (V_i= 20 to 26V)			180 (V_i= 24 to 30V)			200 (V_i= 26 to 32V)			240 (V_i= 30 to 36V)	mV
ΔV_o Load regulation	T_j= 25°C, I_o= 5 mA to 1.5A			300			360			400			480	mV
	T_j= 25°C, I_o= 250 to 750 mA			150			180			200			240	mV
I_d Quiescent current	T_j= 25°C			8			8			8			8	mA
ΔI_d Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
				1 (V_i= 17.5 to 30V)			1 (V_i= 21 to 33V)			1 (V_i= 23 to 35V)			1 (V_i= 27 to 38V)	mA
$\frac{\Delta V_o}{\Delta T}$ Output voltage drift	I_o= 5 mA		-1			-1			-1			-1.5		mV/°C
e_N Output noise voltage	B= 10Hz to 100KHz, T_j= 25°C		90			110			150			170		µV
SVR Supply voltage rejection	f = 120 Hz	54			53			52			50			dB
V_d Dropout voltage	I_o= 1A		2			2			2			2		V
R_o Output resistance	f = 1 KHz		19			22			24			28		mΩ
I_{sc} Short circuit current	V_i= 35V, T_j = 25°C		230			200			180			150		mA
I_{scp} Short circ. peak current	T_j = 25°C		2.1			2.1			2.1			2.1		A

Fig. 4 - Dropout voltage vs. junction temperature

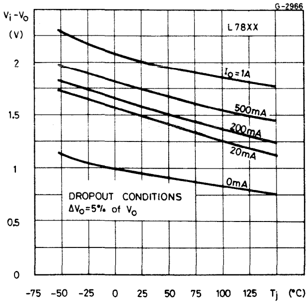


Fig. 5 - Peak output current vs. input/output differential voltage

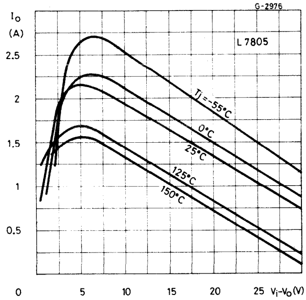


Fig. 6 - Supply voltage rejection vs. frequency

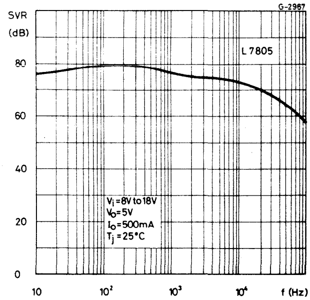


Fig. 7 - Output voltage vs. junction temperature

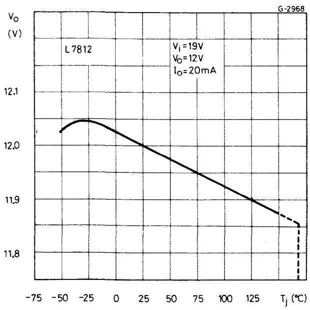


Fig. 8 - Output impedance vs. frequency

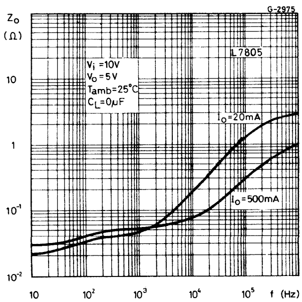


Fig. 9 - Quiescent current vs. junction temperature

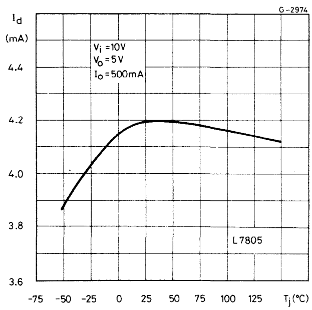


Fig. 10 - Load transient response

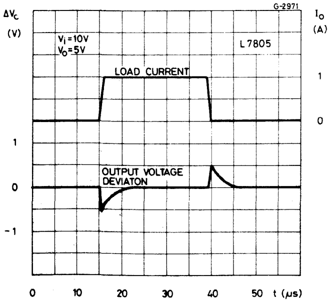


Fig. 11 - Line transient response

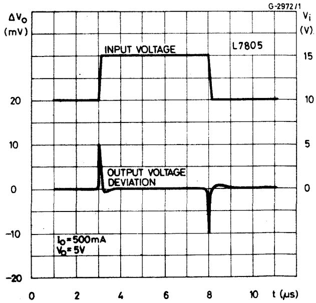
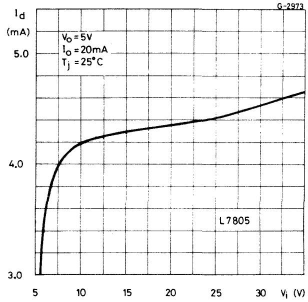
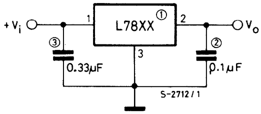


Fig. 12 - Quiescent current vs. input voltage



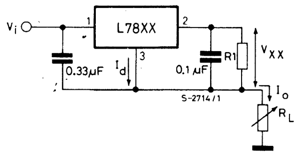
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



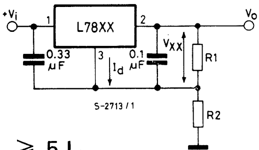
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

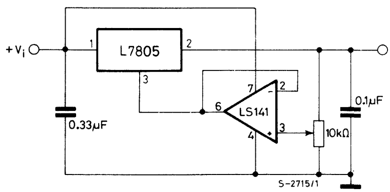
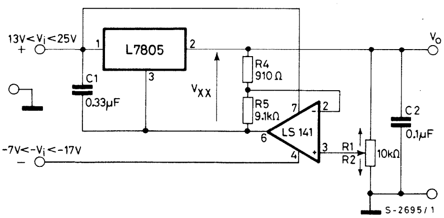
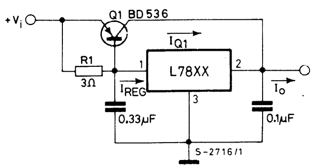


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\,\frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

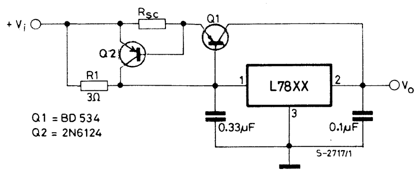


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \dfrac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\left[I_{REG} - \frac{V_{BEQ_1}}{R_1}\right]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

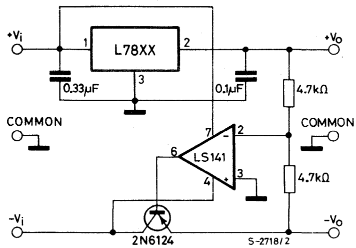
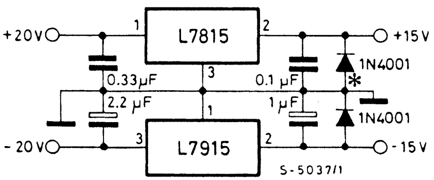


Fig. 21 - Split power supply (±15V - 1A)



* Against potential latch-up problems

Fig. 22 - Negative output voltage circuit

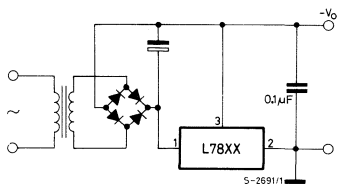


Fig. 23 - Switching regulator

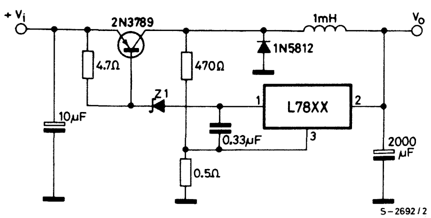
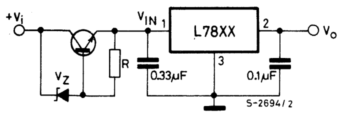


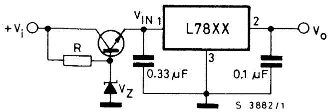
Fig. 24 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

APPLICATION INFORMATION (continued)

Fig. 25 - High input voltage circuit



$$V_{IN} = V_Z - V_{BE}$$

Fig. 26 - High output voltage regulator

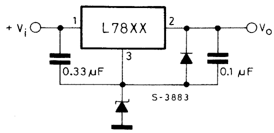
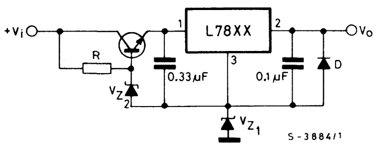
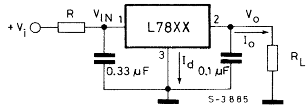


Fig. 27 - High input and output voltage



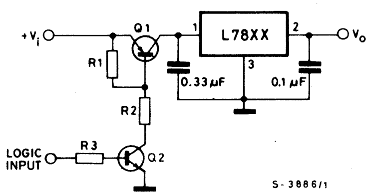
$$V_O = V_{XX} + V_{Z1}$$

Fig. 28 - Reducing power dissipation with dropping resistor



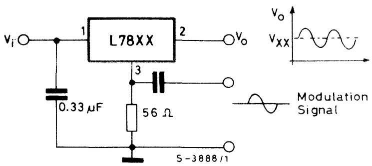
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 29 - Remote shuntdown



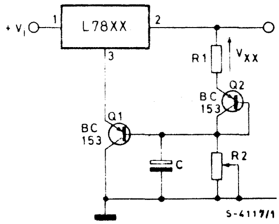
APPLICATION INFORMATION (continued)

Fig. 30 - Power AM modulator (unity voltage gain, $I_o \leqslant 1A$)



Note: The circuit performs well up to 100 KHz.

Fig. 31 - Adjustable output voltage with temperature compensation

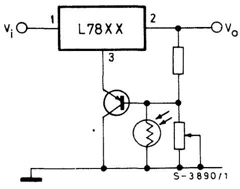


Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX} \left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

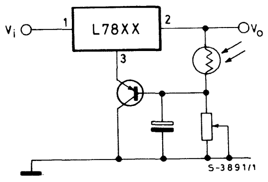
Fig. 32 - Light controllers ($V_{o\ min} = V_{XX} + V_{BE}$)

(a)



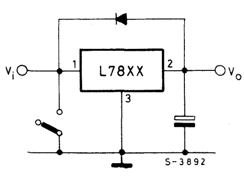
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 33 - Protection against input short-circuit with high capacitance loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

L7800AC Series

LINEAR INTEGRATED CIRCUITS

± 2% POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT IN EXCESS OF 1A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION
- 2% OUTPUT VOLTAGE TOLERANCE

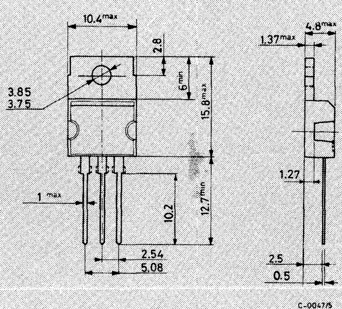
The L7800AC series of three-terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

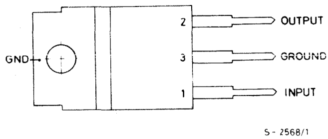
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{op}	Operating junction temperature	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

MECHANICAL DATA

Dimensions in mm

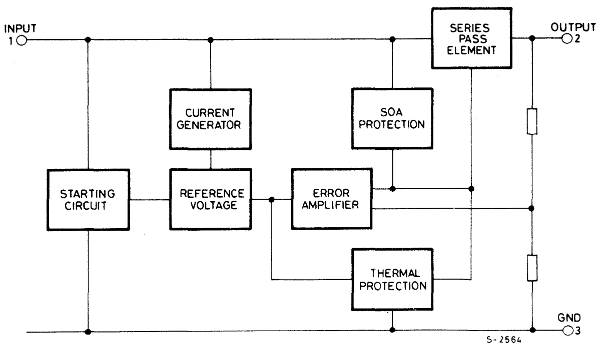


CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)

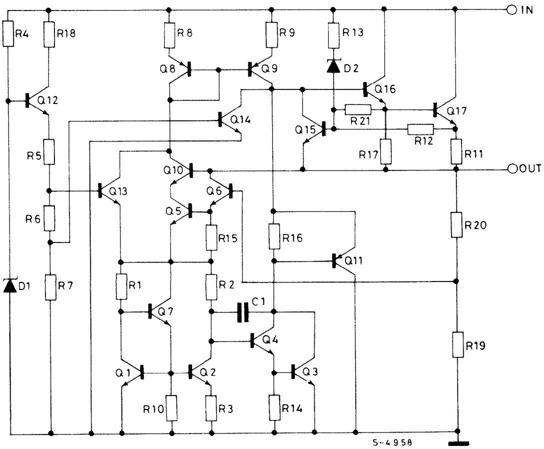


Ordering Numbers	Output Voltage
L7805ACV	5V
L7806ACV	6V
L7808ACV	8V
L7812ACV	12V
L7815ACV	15V
L7818ACV	18V
L7824ACV	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

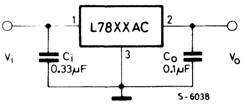


Fig. 2 - Load regulation

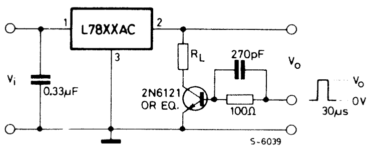
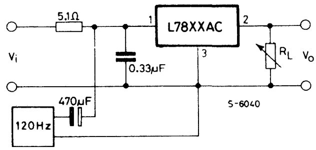


Fig. 3 - Ripple rejection



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

ELECTRICAL CHARACTERISTICS L7805AC (V_i = 10V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	4.9	5	5.1	V
V_o	Output voltage	I_o = 5mA to 1A, Po ≤ 15W V_i = 7.5 to 20V	4.8	5	5.2	V
ΔV_o*	Line regulation	V_i = 7.5 to 25V, I_o = 500 mA V_i = 8 to 12V V_i = 8 to 12V, T_j = 25°C V_i = 7.3 to 20V, T_j = 25°C		7 10 2 7	50 50 25 50	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750 mA		25 25 8	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 8 to 25V, I_o = 500mA V_i = 7.5 to 20V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 8 to 18V, f = 120Hz I_o = 500mA		68		dB
V_d	Dropout voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output noise voltage	f = 10Hz to 100KHz, T_{amb} = 25°C		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		17		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			− 1.1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7806AC (V_i = 11V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	5.88	6	6.12	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 8.6 to 21V	5.76	6	6.24	V
ΔV_o*	Line regulation	V_i = 8.6 to 25V, I_o = 500mA V_i = 9 to 13V V_i = 9 to 13V, T_j = 25°C V_i = 8.3 to 21V, T_j = 25°C		9 11 3 9	60 60 30 60	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, Tj = 25°C I_o = 250 to 750 mA		43 43 16	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 9 to 25V, I_o = 500mA V_i = 8.6 to 21V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 9 to 19V, f = 120Hz I_o = 500mA		65		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_{amb} = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		17		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			−0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7808AC (V_i = 14V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	7.84	8	8.16	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 10.6 to 23V	7.7	8	8.3	V
ΔV_o*	Line regulation	V_i = 10.6 to 25V, I_o = 500mA V_i = 11 to 17V V_i = 11 to 17V, T_j = 25°C V_i = 10.4 to 23V, T_j = 25°C		12 15 5 12	80 80 40 80	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1 A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		45 45 16	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 11 to 25V, I_o = 500mA V_i = 10.6 to 23V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 11.5 to 21.5V, f = 120Hz I_o = 500mA		62		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_{amb} = 25°C, f =10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		18		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			– 0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7812AC (V_i = 19V, I_o = 1A, T_j = 0 to 125°C unles otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	11.75	12	12.25	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 14.8 to 27V	11.5	12	12.5	V
ΔV_o*	Line regulation	V_i = 14.8 to 30V, I_o = 500mA V_i = 16 to 22V V_i = 16 to 22V, T_j = 25°C V_i = 14.5 to 27V, T_j = 25°C		13 16 6 13	120 120 60 120	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		46 46 17	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.4	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 15 to 30V, I_o = 500mA V_i = 14.8 to 27V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 15 to 25V, f = 120Hz I_o = 500mA		60		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_{amb} = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		18		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			−1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7815AC (V_i = 23V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	T_j = 25°C	14.7	15	15.3	V
V_O	Output voltage	I_O = 5mA to 1A, $P_O \leqslant$ 15W V_i = 17.9 to 30V	14.4	15	15.6	V
ΔV_O*	Line regulation	V_i = 17.9 to 30V, I_O = 500mA V_i = 20 to 26V V_i = 20 to 26V, T_j = 25°C V_i = 17.5 to 30V, T_j = 25°C		13 16 6 13	150 150 75 150	mV mV mV mV
ΔV_O*	Load regulation	I_O = 5mA to 1A I_O = 5mA to 1.5 A, T_j = 25°C I_O = 250 to 750 mA		52 52 20	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.4	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 17.5 to 30V, I_O = 500mA V_i = 17.5 to 30V, T_j = 25°C I_O = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 18.5 to 28.5V, f = 120Hz I_O = 500mA		58		dB
V_d	Dropout voltage	I_O = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_{amb} = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_O$
R_O	Output resistance	f = 1KHz		19		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_O}{\Delta T}$	Output voltage drift			− 1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7818AC (V_i = 27V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	17.64	18	18.36	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 21 to 33V	17.3	18	18.7	V
ΔV_o*	Line regulation	V_i = 21 to 33V, I_o = 500mA V_i = 24 to 30V V_i = 24 to 30V, T_j = 25°C V_i = 20.6 to 33V, T_j = 25°C		25 28 10 25	180 180 90 180	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		55 55 22	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.5	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 21 to 33V, I_o = 500mA V_i = 21 to 33V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 22 to 32V, f = 120Hz I_o = 500mA		57		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_{amb} = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		19		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			−1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7824AC (V_i = 33V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	23.5	24	24.5	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 27.3 to 38V	23	24	25	V
ΔV_o*	Line regulation	V_i = 27 to 38V, I_o = 500mA V_i = 30 to 36V V_i = 30 to 36V, T_j = 25°C V_i = 26.7 to 38V, T_j = 25°C		31 35 14 31	240 240 120 240	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1 A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		60 60 25	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.6	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 27.3 to 38V, I_o = 500mA V_i = 27.3 to 38V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 28 to 38V, f = 120Hz I_o = 500mA		54		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_{amb} = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		20		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			-1.5		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

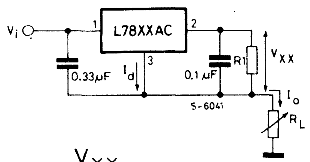
APPLICATIONS INFORMATION

Design Considerations

The L7800AC Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

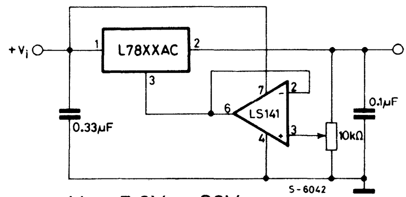
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Fig. 4 - Current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 5 - Adjustable output regulator

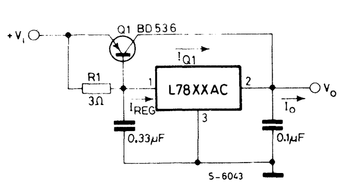


V_O, 7.0V to 20V

$V_i - V_O \geqslant 2.0V$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0V greater than the regulator voltage.

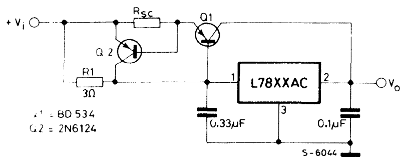
Fig. 6 - Current boost regulator



$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1} \left[I_{REG} - \frac{V_{BEQ_1}}{R_1} \right]$$

Fig. 7 - Short-circuit protection



The circuit of Figure 6 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

LINEAR INTEGRATED CIRCUITS

L78M00 Series

PRELIMINARY DATA

POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 0.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

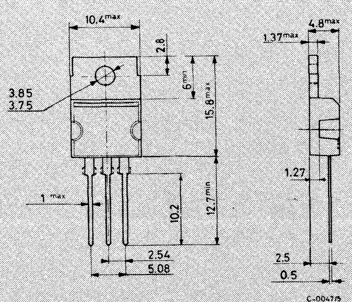
The L78M00 series of three-terminal positive regulators is available in TO-220 and SOT-82 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

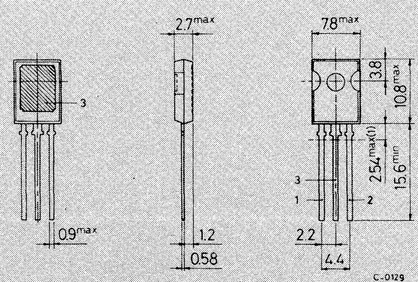
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_{op}	Operating junction temperature	0 to +150	°C

MECHANICAL DATA

Dimensions in mm



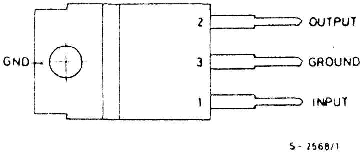
TO-220



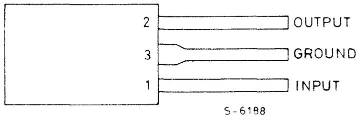
(1) Within this region the cross-section of the leads is uncontrolled

SOT-82

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



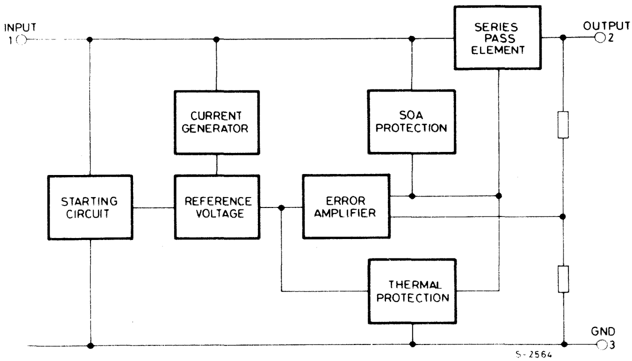
TO-220



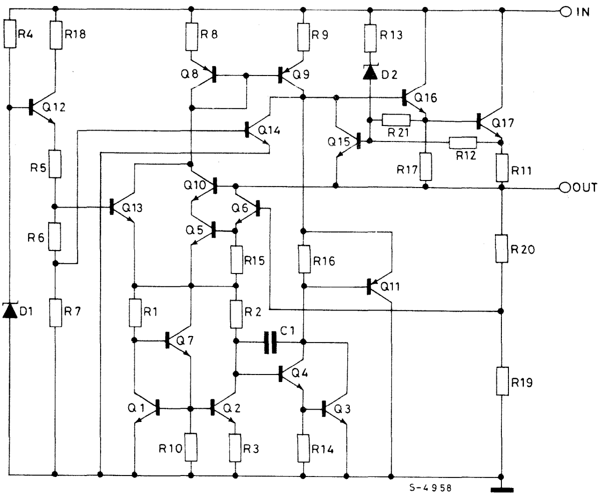
SOT-82

Ordering Numbers		Output Voltage
TO-220	SOT-82	
L78M05CV	L78M05CX	5V
L78M06CV	L78M06CX	6V
L78M08CV	L78M08CX	8V
L78M12CV	L78M12CX	12V
L78M15CV	L78M15CX	15V
L78M18CV	L78M18CX	18V
L78M20CV	L78M20CX	20V
L78M24CV	L78M24CX	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

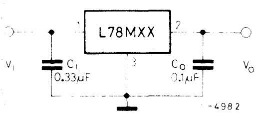


Fig. 2 - Load regulation

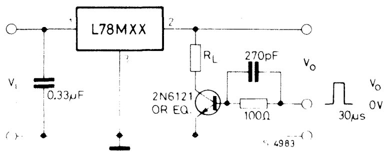
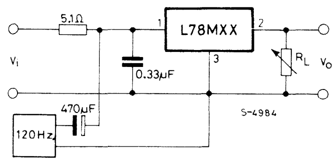


Fig. 3 - Ripple rejection



THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W	50 °C/W

L78M00 Series

ELECTRICAL CHARACTERISTICS L78M00C (Refer to the test circuits, $T_j = 25°C$, $I_o = 350$ mA unless otherwise specified, $C_i = 0.33\ \mu F$, $C_o = 0.1\ \mu F$)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o = 5 to 350 mA	4.75	5	5.25	5.7	6	6.3	7.6	8	8.4	11.4	12	12.6	V
				(V_i = 7 to 20V)			(V_i = 8 to 21V)			(V_i = 10.5 to 23V)			(V_i = 14.5 to 27V)		
ΔV_o	Line regulation	I_o = 200 mA			100			100			100			100	mV
				(V_i = 7 to 25V)			(V_i = 8 to 25V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 30V)		
					50			50			50			50	mV
				(V_i = 8 to 25V)			(V_i = 9 to 25V)			(V_i = 11 to 25V)			(V_i = 16 to 30V)		
ΔV_o	Load regulation	I_o = 5 mA to 0.5A			100			120			160			240	mV
		I_o = 5 mA to 200 mA			50			60			80			120	mV
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_o = 200 mA			0.8			0.8			0.8			0.8	mA
				(V_i = 8 to 25V)			(V_i = 9 to 25V)			(V_i = 10.5 to 25)			(V_i = 14.5 to 30V)		
$\frac{\Delta V_o}{\Delta T}$	Output Voltage drift	I_o = 5 mA T_j = 0 to 125°C		-0.5			-0.5			-0.5			-1.0		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz		40			45			52			75		μV
SVR	Supply voltage rejection	f = 120 Hz I_o = 300 mA	62			59			56			55			dB
				(V_i = 8 to 18V)			(V_i = 9 to 19V)			(V_i=11.5 to 21.5V)			(V_i = 15 to 25V)		
V_d	Dropout voltage			2			2			2			2		V
I_{sc}	Short circuit current	V_i = 35V		300			270			250			240		mA
I_{scp}	Short circ. peak current			700			700			700			700		mA

ELECTRICAL CHARACTERISTICS L78M00C (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			29			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage		14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_O= 5 to 350 mA	14.25 (Vi= 17.5 to 30V)	15	15.75	17.1 (V_i= 20.5 to 33V)	18	18.9	19 (V_i= 23 to 35V)	20	21	22.8 (V_i= 27 to 38V)	24	25.2	V
ΔV_O	Line regulation	I_O= 200 mA			100 (V_i= 17.5 to 30V)			100 (V_i= 21 to 33V)			100 (V_i= 23 to 35V)			100 (V_i= 27 to 38V)	mV
					50 (V_i= 20 to 30V)			50 (V_i= 24 to 33V)			50 (V_i= 24 to 35V)			50 (V_i= 28 to 38V)	mV
ΔV_O	Load regulation	I_O= 5 mA to 0.5A			300			360			400			480	mV
		I_O= 5 mA to 200 mA			150			180			200			240	mV
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	I_O= 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_O= 200 mA			0.8 (V_i= 17.5 to 30V)			0.8 (V_i= 21 to 33V)			0.8 (V_i= 23 to 35V)			0.8 (V_i= 27 to 38V)	mA
$\frac{\Delta V_O}{\Delta T}$	Output voltage drift	I_O= 5 mA, T_{amb}= 0 to 125°C		-1			-1.1			-1.1			-1.2		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		90			100			110			170		µV
SVR	Supply voltage rejection	f = 120 Hz, I_O= 300 mA	54 (V_i= 18.5 to 28.5V)			53 (V_i= 22 to 32V)			53 (V_i= 24 to 34V)			50 (V_i= 28 to 38V)			dB
V_d	Dropout Voltage			2			2			2			2		V
I_{sc}	Short circuit current	V_i= 35V		240			240			240			240		mA
I_{scp}	Short circ. peak current			700			700			700			700		mA

L78M00 Series

Fig. 4 - Dropout voltage vs. junction temperature

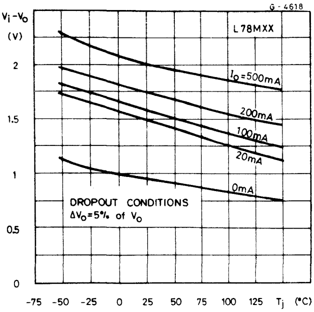


Fig. 5 - Dropout characteristics

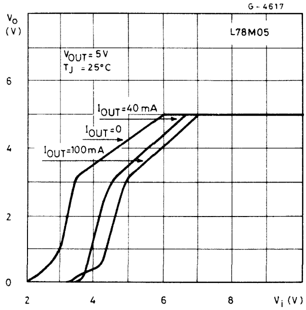


Fig. 6 - Peak output current vs. input-output differential voltage

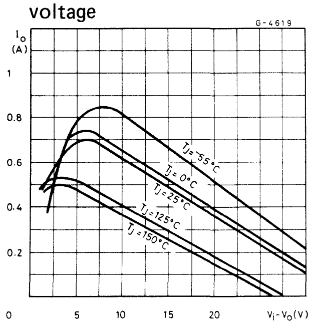


Fig. 7 - Output voltage vs. junction temperature

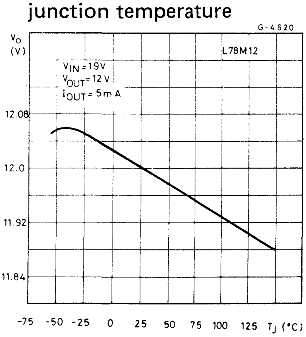


Fig. 8 - Supply voltage rejection vs. frequency

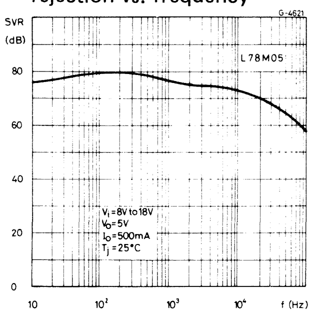


Fig. 9 - Quiescent current vs. junction temperature

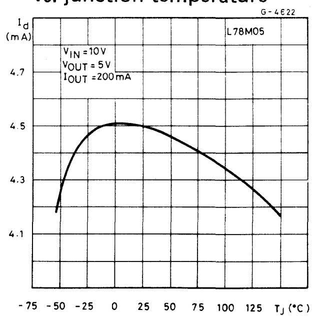


Fig. 10 - Load transient response

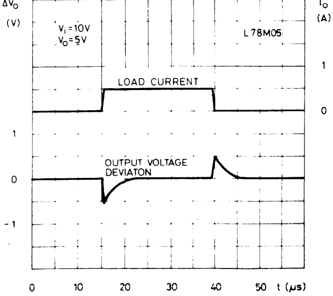


Fig. 11 - Line transient response

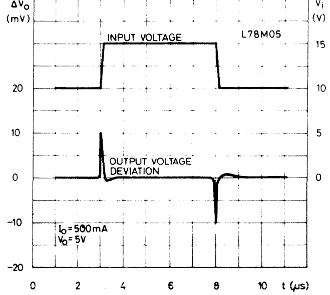
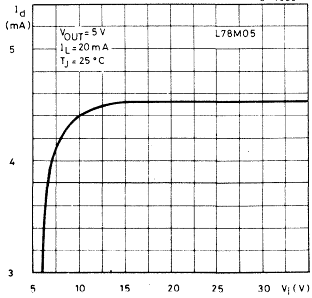
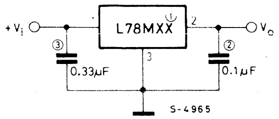


Fig. 12 - Quiescent current vs. input voltage



APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



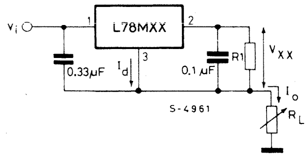
Notes:

(1) To specify an output voltage, substitute voltage value for "XX".

(2) Although no output capacitor is needed for stability, it does improve transient response.

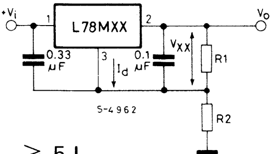
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

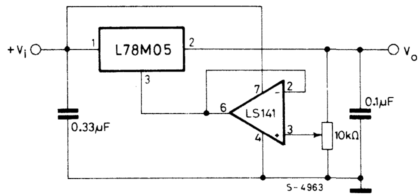
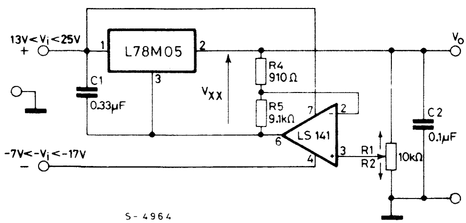
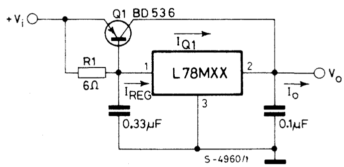


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\,\frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

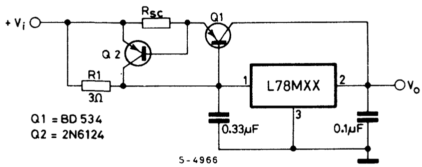


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \dfrac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\left[I_{REG} - \frac{V_{BEQ_1}}{R_1}\right]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

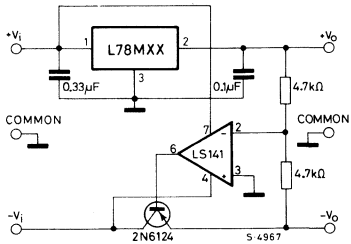
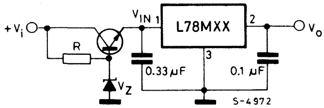
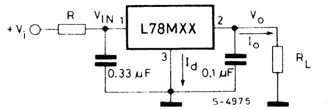


Fig. 21 - High input voltage circuit



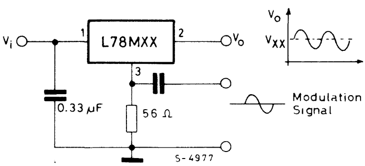
$$V_{IN} = V_Z - V_{BE}$$

Fig. 22 - Reducing power dissipation with dropping resistor



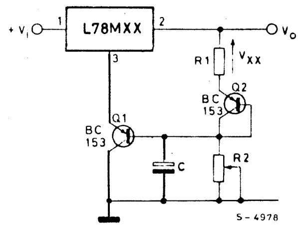
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 23 - Power AM modulator (unity voltage gain, $I_o \leqslant 0.5$)



Note: The circuit performs well up to 100 KHz.

Fig. 24 - Adjustable output voltage with temperature compensation



Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

L78S00 Series

LINEAR INTEGRATED CIRCUITS

2A POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 2A
- OUTPUT VOLTAGES OF 5; 7.5; 9; 10; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

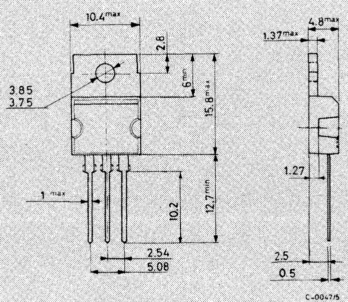
The L78S00 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 2A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

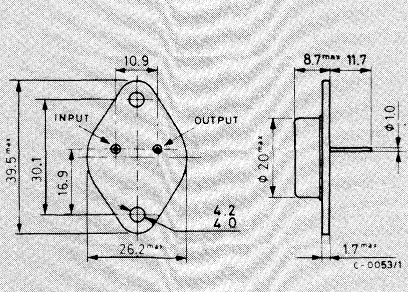
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_{op}	Operating junction temperature (for **L78S00**)	-55 to +150	°C
	(for **L78S00C**)	0 to +150	°C

MECHANICAL DATA

Dimensions in mm

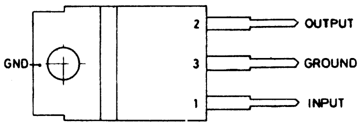


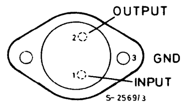
TO-220



TO-3

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

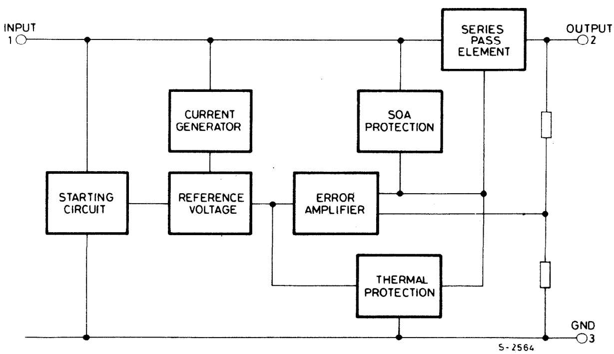




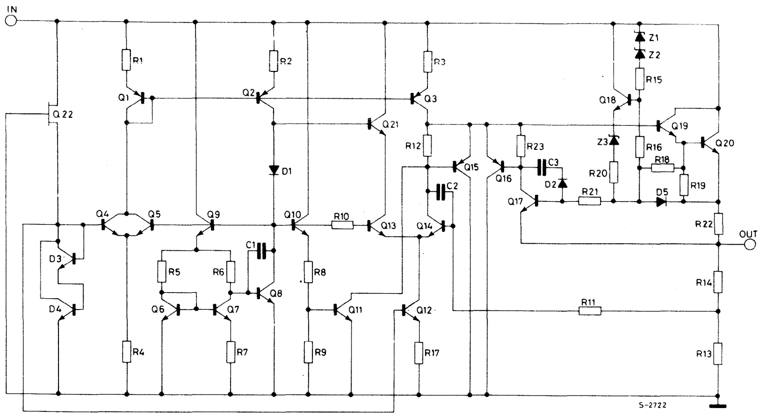
S-2568/1

Type	TO-220	TO-3	Output voltage
L 78S05	–	L 78S05T	5V
L 78S05C	L 78S05CV	L 78S05CT	5V
L 78S75	–	L 78S75T	7.5V
L 78S75C	L 78S75CV	L 78S75CT	7.5V
L 78S09	–	L 78S09T	9V
L 78S09C	L 78S09CV	L 78S09CT	9V
L 78S10	–	L 78S10T	10V
L 78S10C	L 78S10CT	L 78S10CT	10V
L 78S12	–	L 78S12T	12V
L 78S12C	L 78S12CV	L 78S12CT	12V
L 78S15	–	L 78S15T	15V
L 78S15C	L 78S15CV	L 78S15CT	15V
L 78S18	–	L 78S18T	18V
L 78S18C	L 78S18CV	L 78S18CT	18V
L 78S24	–	L 78S24T	24V
L 78S24C	L 78S24CV	L 78S24CT	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

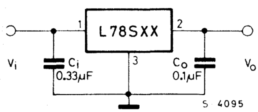


Fig. 2 - Load regulation

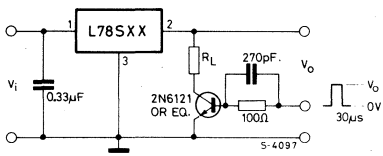
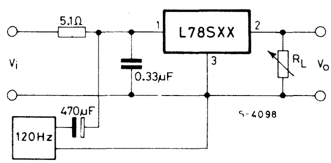


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L78S00 (Refer to the test circuits, T_j = 25°C, I_o = 500 mA unless otherwise specified)

OUTPUT VOLTAGE			5			7.5			9			10			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			12.5			14			15			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		I_o = 1A	4.75	5 (V_i = 7V)	5.25	7.1	7.5 (V_i = 9.5V)	7.95	8.6	9 (V_i = 11V)	9.4	9.4	10 (V_i = 12.5V)	10.6	V
ΔV_o	Line regulation				100 (V_i = 7 to 25V)			120 (V_i = 9.5 to 25V)			130 (V_i = 11 to 25V)			200 (V_i = 12.5 to 30V)	mV
					50 (V_i = 8 to 12V)			60 (V_i = 10.5 to 20V)			65 (V_i = 11 to 20V)			100 (V_i = 14 to 22V)	mV
ΔV_o	Load regulation	I_o = 20 mA to 2A			100			120			130			150	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o = 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o = 20 mA			1.3 (V_i = 7 to 25V)			1.3 (V_i = 9.5 to 25V)			1.3 (V_i = 11 to 25V)			1 (V_i = 12.5 to 30V)	mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 5 mA T_j = -55 to 150°C		-1.1			-0.8			-1			-1		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz		40			52			60			65		µV
SVR	Supply voltage rejection	f = 120 Hz	60			54			53			53			dB
V_i	Operating input voltage	$I_o \leq$ 1.5A	8			10.5			12			13			V
R_o	Output resistance	f = 1 KHz		17			16			17			17		mΩ
I_{sc}	Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short circ. peak current				3.5			3.5			3.5			3.5	A

ELECTRICAL CHARACTERISTICS L78S00 (continued)

OUTPUT VOLTAGE		12			15			18			24			Unit
INPUT VOLTAGE (Unless otherwise specified)		19			23			26			33			
Parameter	Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o Output voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
	I_o = 1A	11.4	12	12.6	14.25	15	15.75	17	18	19	22.8	24	25.2	V
		(V_i = 14.5V)			(V_i = 17.5V)			(V_i = 20.5V)			(V_i = 27V)			
ΔV_o Line regulation				240 (V_i = 14.5 to 30V)			300 (V_i = 17.5 to 30V)			360 (V_i = 20.5 to 30V)			480 (V_i = 27 to 38V)	mV
				120 (V_i = 16 to 22V)			150 (V_i = 20 to 26V)			180 (V_i = 22 to 28V)			240 (V_i = 30 to 36V)	mV
ΔV_o Load regulation	I_o = 20 mA to 2A			160			180			200			250	mV
I_d Quiescent current				8			8			8			8	mA
ΔI_d Quiescent current change	I_o = 20 mA to 1A			0.5			0.5			0.5			0.5	mA
	I_o = 20 mA			1 (V_i = 14.5 to 30V)			1 (V_i = 17.5 to 30V)			1 (V_i = 22 to 33V)			1 (V_i = 28 to 38V)	mA
$\frac{\Delta V_o}{\Delta T}$ Output voltage drift	I_o = 5mA T_{amb} = 0 to 70°C		-1			-1			-1			-1.5		mV/°C
e_N Output noise voltage	B = 10Hz to 100KHz		75			90			110			170		µV
SVR Supply voltage rejection	f = 120 Hz	53			52			49			48			dB
V_i Operating input voltage	$I_o \leq$ 1.5A	15			18			21			27			V
R_o Output resistance	f = 1 KHz		18			19			22			23		mΩ
I_{sc} Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp} Short circ. peak current				3.5			3.5			3.5			3.5	A

ELECTRICAL CHARACTERISTICS L78S00C (Refer to the test circuits, $T_j = 25°C$, $I_o = 500mA$ unless otherwise specified)

OUTPUT VOLTAGE			5			7.5			9			10			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			12.5			14			15			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		$I_o = 1A$	4.75	5	5.25	7.1	7.5	7.95	8.6	9	9.4	9.4	10	10.6	V
				($V_i = 7V$)			($V_i = 9.5V$)			($V_i = 11V$)			($V_i = 12.5V$)		
ΔV_o	Line regulation				100			120			130			200	mV
					($V_i = 7$ to $25V$)			($V_i = 9.5$ to $25V$)			($V_i = 11$ to $25V$)			($V_i = 12.5$ to $30V$)	
					50			60			65			100	mV
					($V_i = 8$ to $12V$)			($V_i = 10.5$ to $20V$)			($V_i = 11$ to $20V$)			($V_i = 14$ to $22V$)	
ΔV_o	Load regulation	$I_o = 20$ mA to 2A			100			140			170			240	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	$I_o = 20$ mA to 1A			0.5			0.5			0.5			0.5	mA
		$I_o = 20$ mA			1.3			1.3			1.3			1.0	mA
					($V_i = 7$ to $25V$)			($V_i = 9.5$ to $25V$)			($V_i = 11$ to $25V$)			($V_i = 12.5$ to $30V$)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	$I_o = 5$ mA, $T_{amb} = 0$ to $70°C$		-1.1			-0.8			-1			-1		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		40			52			60			65		µV
SVR	Supply voltage rejection	f = 120 Hz	54			48			47			47			dB
V_i	Operating input voltage	$I_o \leq 1.5A$	8			10.5			12			13			V
R_o	Output resistance	f = 1 KHz		17			16			17			17		mΩ
I_{sc}	Short circuit current	$V_i = 27V$		500			500			500			500		mA
I_{scp}	Short circ. peak current				3.5			3.5			3.5			3.5	A

ELECTRICAL CHARACTERISTICS L78S00C (continued)

OUTPUT VOLTAGE			12			15			18			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			19			23			26			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
		I_o= 1A	11.4	12 (V_i= 14.5V)	12.6	14.25	15 (V_i= 17.5V)	15.75	17	18 (V_i= 20.5V)	19	22.8	24 (V_i= 27V)	25.2	V
ΔV_o	Line regulation				240 (V_i= 14.5 to 30V)			300 (V_i= 17.5 to 30V)			360 (V_i= 20.5 to 30V)			480 (V_i= 27 to 38V)	mV
					120 (V_i= 16 to 22V)			150 (V_i= 20 to 26V)			180 (V_i= 22 to 28V)			240 (V_i= 30 to 36V)	mV
ΔV_o	Load regulation	I_o= 20 mA to 2A			240			300			360			480	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1.0 (V_i = 14.5 to 30V)			1.0 (V_i = 17.5 to 30V			1.0 (V_i = 20.5 to 30V)			1.0 (V_i = 27 to 38V)	mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5mA T_{amb}= 0 to 70°C		-1			-1			-1			-1.5		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		75			90			110			170		µV
SVR	Supply voltage rejection	f = 120 Hz	47			46			43			42			dB
V_i	Operating input voltage	$I_o \leq$ 1.5A	15			18			21			27			V
R_o	Output resistance	f = 1 KHz		18			19			22			28		mΩ
I_{sc}	Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short circ. peak current				3.5			3.5			3.5			3.5	A

Fig. 4 - Dropout voltage vs. junction temperature

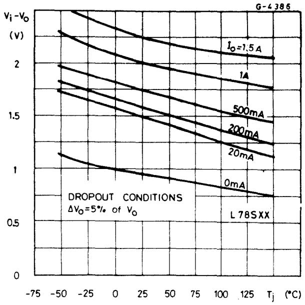


Fig. 5 - Peak output current vs. input/output differential voltage

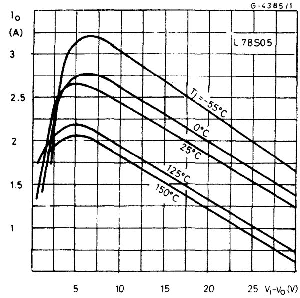


Fig. 6 - Supply voltage rejection vs. frequency

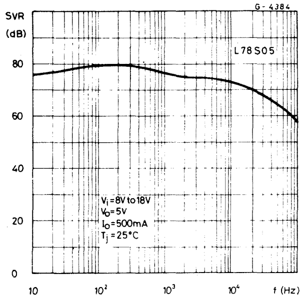


Fig. 7 - Output voltage vs. junction temperature

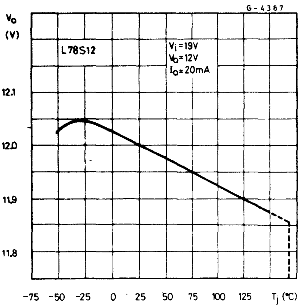


Fig. 8 - Output impedance vs. frequency

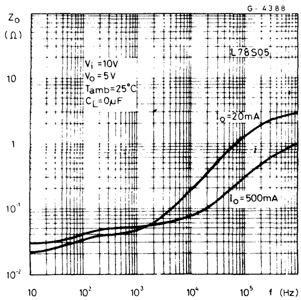


Fig. 9 - Quiescent current vs. junction temperature

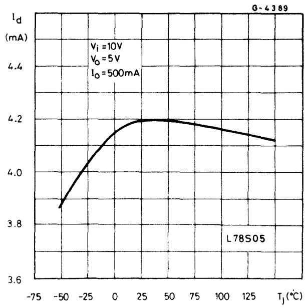


Fig. 10 - Load transient response

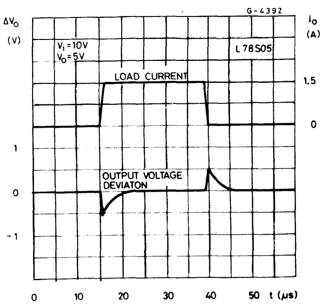


Fig. 11 - Line transient response

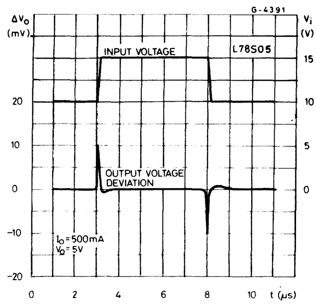
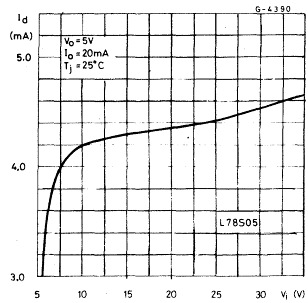
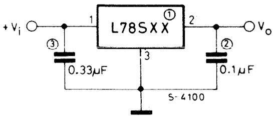


Fig. 12 - Quiescent current vs. input voltage



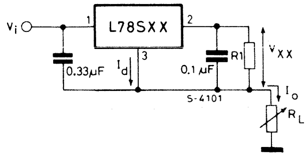
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



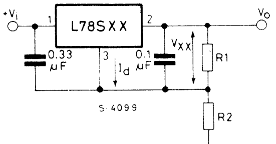
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

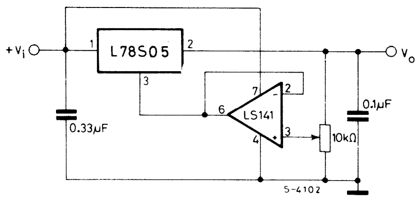
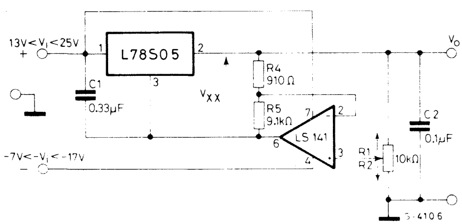
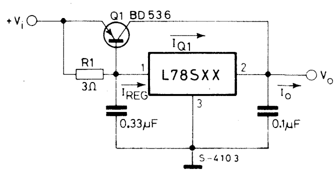


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\,\frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

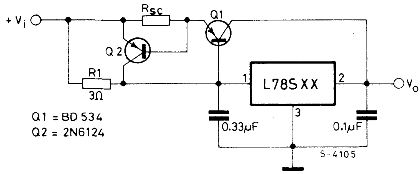


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \dfrac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\left[I_{REG} - \frac{V_{BEQ_1}}{R_1}\right]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

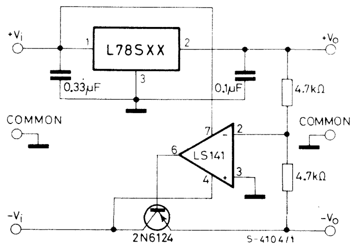
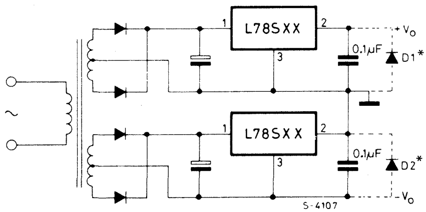


Fig. 21 - Positive and negative regulator



(*) D_1 and D_2 are necessary if the load is connected between $+V_o$ and $-V_o$

Fig. 22 - Negative output voltage circuit

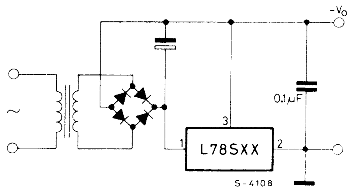


Fig. 23 - Switching regulator

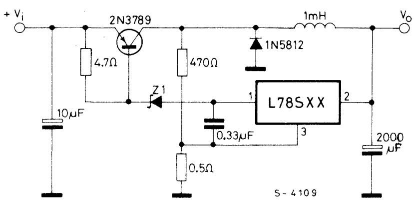
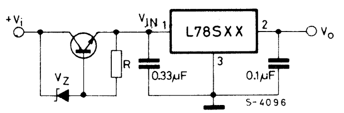


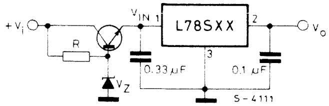
Fig. 24 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

APPLICATION INFORMATION (continued)

Fig. 25 - High input voltage circuit



$V_{IN} = V_Z - V_{BE}$

Fig. 26 - High output voltage regulator

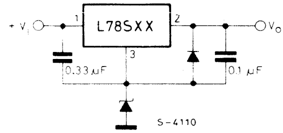
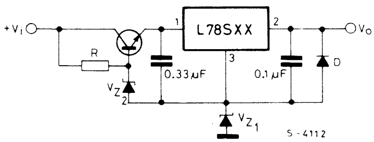
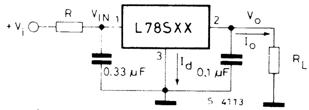


Fig. 27 - High input and output voltage



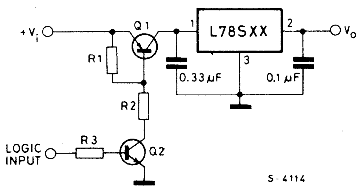
$V_O = V_{XX} + V_{Z1}$

Fig. 28 - Reducing power dissipation with dropping resistor



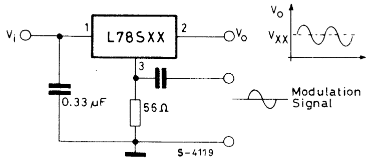
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 29 - ·Remote shuntdown



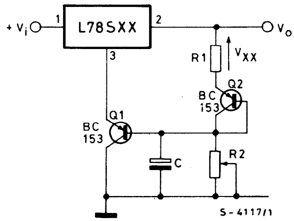
APPLICATION INFORMATION (continued)

Fig. 30 - Power AM modulator oscillator (unity voltage gain, $I_o \leqslant 1.5A$)



Note: The circuit performs well up to 100 KHz.

Fig. 31 - Adjustable output voltage with temperature compensation

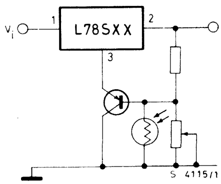


Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

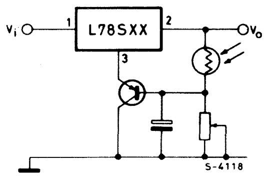
Fig. 32 - Light controllers ($V_{o\,min} = V_{XX} + V_{BE}$)

(a)



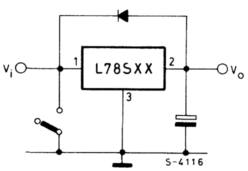
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 33 - Protection against input short-circuit with high capacitance loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

LINEAR INTEGRATED CIRCUITS

L7900 Series

PRELIMINARY DATA

NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF -5; -5.2; -8; -12; -15; -18; -20; -24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

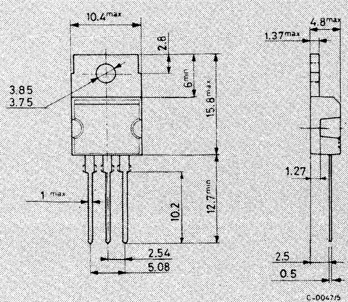
The L7900 series of three-terminal negative regulators is available in TO-220 and TO-3 packages and with several output voltages. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the -5.2V is also available for ECL system.
If adeguate heatsinking is provided, the L7900 series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

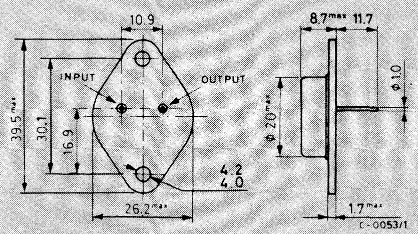
V_i	DC input voltage (for V_o = -5 to -18V)	-35	V
	(for V_o = -20, -24V)	-40	V
I_o	Output current	Internally limited	
P_{tot}	Total power dissipation	Internally limited	
T_{op}	Operating junction temperature	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

MECHANICAL DATA

Dimensions in mm

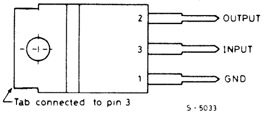


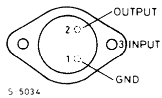
TO-220



TO-3

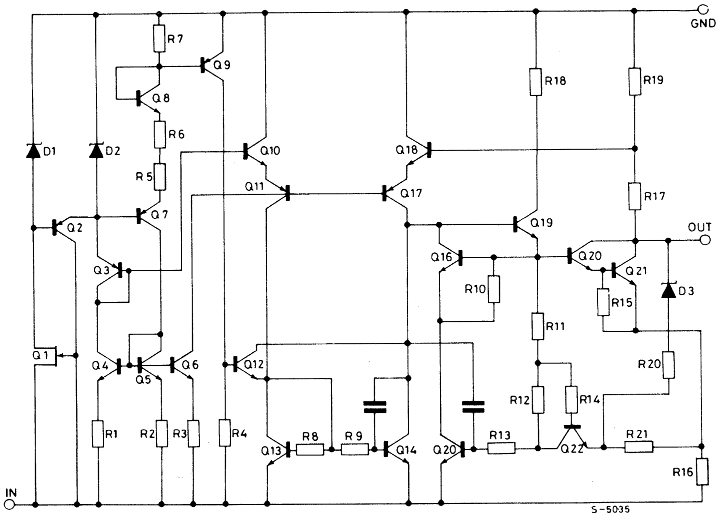
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-220	TO-3	Output Voltage
L7905C	L7905CV	L7905CT	-5V
L7952C	L7952CV	L7952CT	-5.2V
L7908C	L7908CV	L7908CT	-8V
L7912C	L7912CV	L7912CT	-12V
L7915C	L7915CV	L7915CT	-15V
L7918C	L7918CV	L7918CT	-18V
L7920C	L7920CV	L7920CT	-20V
L7924C	L7924CV	L7924CT	-24V

SCHEMATIC DIAGRAM



THERMAL DATA			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L7900C (C_i = 2.2 µF, C_o = 1 µF, T_j = 0 to 125°C, I_o = 500 mA unless otherwise specified)

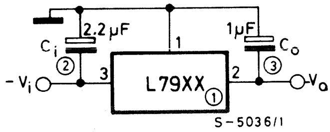
OUTPUT VOLTAGE			-5			-5.2			-8			-12			Unit
INPUT VOLTAGE (Unless otherwise specified)			-10			-10			-14			-19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	-4.8	-5	-5.2	-5	-5.2	-5.4	-7.7	-8	-8.3	-11.5	-12	-12.5	V
		I_o = 5 mA to 1A P_o < 15W	-4.75	-5	-5.25 (V_i = -8 to -20V)	-4.95	-5.2	-5.45 (V_i = -9 to -21V)	-7.6	-8	-8.4 (V_i = -11.5 to -23V)	-11.4	-12	-12.6 (V_i = -15.5 to -27V)	V
ΔV_o	Line regulation	T_j = 25°C			100 (V_i = -7 to -25V)			105 (V_i = -8 to -25V)			160 (V_i = -10.5 to -25V)			240 (V_i = -14.5 to -30V)	mV
					50 (V_i = -8 to -12V)			52 (V_i = -9 to -13V)			80 (V_i = -11 to -17V)			120 (V_i = -16 to -22V)	mV
ΔV_o	Load regulation	T_j = 25°C I_o = 5 mA to 1.5A			100			105			160			240	mV
		T_j = 25°C I_o = 250 to 750 mA			50			52			80			120	mV
I_d	Quiescent current	T_j = 25°C			2			2			2			3	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3 (V_i = -8 to -25V)			1.3 (V_i = -9 to -25V)			1 (V_i = -11.5 to -25V)			1 (V_i = -15 to -30V)	mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 5 mA		-0.4			-0.5			-0.6			-0.8		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz T_j = 25°C		100			125			175			200		µV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i = 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j = 25°C I_o = 1A ΔV_o = 100 mV		2			1.8			1.1			1.1		V
I_{sc}	Short circuit current			2.1			2			1.5			1.5		A
I_{scp}	Short circ. peak current	T_j = 25°C		2.5			2.5			2.5			2.5		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE			-15			-18			-20			-24			Unit
INPUT VOLTAGE (Unless otherwise specified)			-23			-27			-29			-33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	-14.4	-15	-15.6	-17.3	-18	-18.7	-19.2	-20	-20.8	-23	-24	-25	V
		I_o= 5 mA to 1A P_o < 15W	-14.3	-15	-15.7 (V_i=-18.5 to -30V)	-17.1	-18	-18.9 (V_i= -22 to -33V)	-19	-20	-21 (V_i= -24 to -35V)	-22.8	-24	-25.2 (V_i= -27 to -38V)	V
ΔV_o	Line regulation	T_j = 25°C			300 (V_i=-17.5 to -30V)			360 (V_i= -21 to -33V)			400 (V_i= -23 to -35V)			480 (V_i= -27 to -38V)	mV
					150 (V_i= -20 to -26V)			180 (V_i= -24 to -30V)			200 (V_i= -26 to -32V)			240 (V_i= -30 to -36V)	mV
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			300			360			400			480	mV
		T_j= 25°C I_o= 250 to 750 mA			150			180			200			240	mV
I_d	Quiescent current	T_j= 25°C			3			3			3			3	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1 (V_i=-18.5 to -30V)			1 (V_i= -22 to -33V)			1 (V_i= -24 to -35V)			1 (V_i= -27 to -38V)	mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-0.9			-1			-1.1			-1		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz T_j= 25°C		250			300			350			400		µV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j= 25°C I_o= 1A ΔV_o= 100 mV		1.1			1.1			1.1			1.1		V
I_{sc}	Short circuit current			1.3			1.1			0.9			1.1		A
I_{scp}	Short circ. peak current	T_j= 25°C		2.2			2.2			2.2			2.2		A

APPLICATION INFORMATION

Fig. 1 - Fixed output regulator



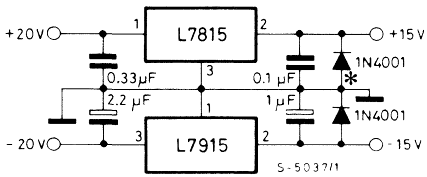
Notes:

(1) To specify an output voltage, substitute voltage value for "XX".

(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.

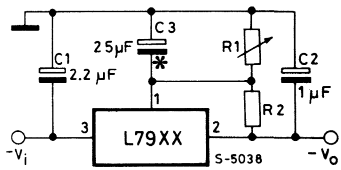
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 - Split power supply (± 15V/1A)



* Against potential latch-up problems.

Fig. 3 - Circuit for increasing output voltage



$$V_o \cong V_{xx} \cdot \frac{R1 + R2}{R2} \qquad \frac{V_{xx}}{R2} > 3\, I_d$$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 - High current negative regulator (-5V/4A with 5A current limiting)

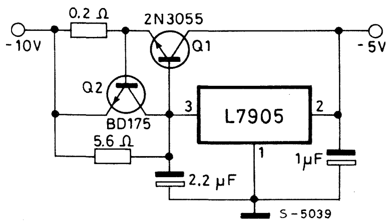
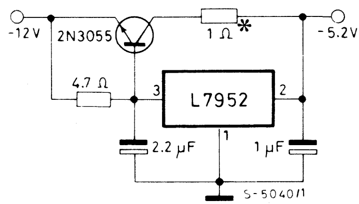


Fig. 5 - Typical ECL system power supply (-5.2V/ 4A)



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

L7900AC Series

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

± 2% NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF -5; -5.2; -8; -12; -15; -18; -20; -24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

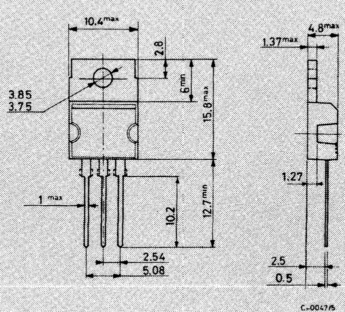
The L7900 AC series of three-terminal negative regulators is available in TO-220 package and with several output voltage. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the -5.2V is also available for ECL system.
If adeguate heatsinking is provided, the L7900 AC series can deliver an output current in excess of 1.5A. Althrough designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

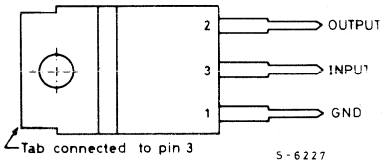
V_i	DC input voltage (for V_o = -5 to -18V)	-35	V
	(for V_o = -20, -24V)	-40	V
I_o	Output current	Internally limited	
P_{tot}	Total power dissipation	Internally limited	
T_{op}	Operating junction temperature	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

MECHANICAL DATA

Dimensions in mm

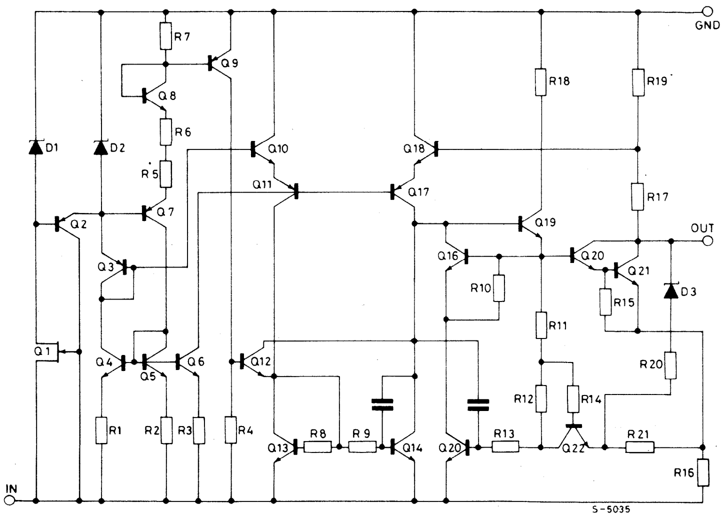


CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



Ordering Numbers	Output Voltage
L7905ACV	-5V
L7952ACV	-5.2V
L7908ACV	-8V
L7912ACV	-12V
L7915ACV	-15V
L7918ACV	-18V
L7920ACV	-20V
L7924ACV	-24V

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W

ELECTRICAL CHARACTERISTICS L7900AC (C_i = 2.2 μF, C_o = 1 μF, T_j = 0 to 125°C, I_o = 500 mA unless otherwise specified)

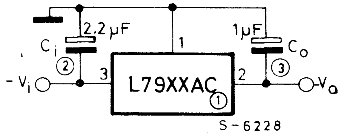
OUTPUT VOLTAGE		-5			-5.2			-8			-12			Unit
INPUT VOLTAGE (Unless otherwise specified)		-10			-10			-14			-19			
Parameter	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	
V_o Output voltage	T_j = 25°C	-4.9	-5	-5.1	-5.1	-5.2	-5.3	-7.84	-8	-8.16	-11.75	-12	-12.25	V
	I_o = 5 mA to 1A, P_o < 15W	-4.8	-5 (V_i = -8 to -20V)	-5.2	-5.0	-5.2 (V_i = -9 to -21V)	-5.4	-7.7	-8 (V_i = -11.5 to -23V)	-8.3	-11.5	-12 (V_i = -15.5 to -27V)	-12.5	V
ΔV_o Line regulation	T_j = 25°C			100 (V_i = -7 to -25V)			105 (V_i = -8 to -25V)			160 (V_i = -10.5 to -25V)			240 (V_i = -14.5 to -30V)	mV
	T_j = 25°C			50 (V_i = -8 to -12V)			52 (V_i = -9 to -13V)			80 (V_i = -11 to -17V)			120 (V_i = -16 to -22V)	mV
ΔV_o Load regulation	T_j = 25°C, I_o = 5 mA to 1.5A			100			105			160			240	mV
	T_j = 25°C, I_o = 250 to 750 mA			50			52			80			120	mV
I_d Quiescent current	T_j = 25°C			2			2			2			3	mA
ΔI_d Quiescent current change	I_o = 5 mA to 1A			0.5			0.5			0.5			0.5	mA
				1.3 (V_i = -8 to -25V)			1.3 (V_i = -9 to -25V)			1 (V_i = -11.5 to -25V)			1 (V_i = -15 to -30V)	mA
$\frac{\Delta V_o}{\Delta T}$ Output voltage drift	I_o = 5 mA		-0.4			-0.5			-0.6			-0.8		mV/°C
e_N Output noise voltage	B = 10Hz to 100KHz, T_j = 25°C		100			125			175			200		μV
SVR Supply voltage rejection	f = 120 Hz, ΔV_i = 10V	54	60		54	60		54	60		54	60		dB
V_{i-o} Dropout voltage	T_j = 25°C, I_o = 1A, ΔV_o = 100 mV		2			1.8			1.1			1.1		V
I_{sc} Short circuit current			2.1			2			1.5			1.5		A
I_{scp} Short circ. peak current	T_j = 25°C		2.5			2.5			2.5			2.5		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE		-15			-18			-20			-24			Unit
INPUT VOLTAGE (Unless otherwise specified)		-23			-27			-29			-33			
Parameter	Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o Output voltage	T_j = 25°C	-14.7	-15	-15.3	-17.64	-18	-18.36	-19.6	-20	-20.4	-23.5	-24	-24.5	V
	I_o= 5 mA to 1A, P_o < 15W	-14.4 (Vi=-18.5 to -30V)	-15	-15.6	-17.3 (V_i= -22 to -33V)	-18	-18.7	-19.4 (V_i= -24 to -35V)	-20	-20.8	-23 (V_i= -27 to -38V)	-24	-25	V
ΔV_o Line regulation	T_j = 25°C			300 (V_i=-17.5 to -30V)			360 (V_i= -21 to -33V)			400 (V_i= -23 to -35V)			480 (V_i= -27 to -38V)	mV
				150 (V_i= -20 to -26V)			180 (V_i= -24 to -30V)			200 (V_i= -26 to -32V)			240 (V_i= -30 to -36V)	mV
ΔV_o Load regulation	T_j= 25°C, I_o= 5 mA to 1.5A			300			360			400			480	mV
	T_j= 25°C, I_o= 250 to 750 mA			150			180			200			240	mV
I_d Quiescent current	T_j= 25°C			3			3			3			3	mA
ΔI_d Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
				1 (V_i=-18.5 to -30V)			1 (V_i= -22 to -33V)			1 (V_i= -24 to -35V)			1 (V_i= -27 to -38V)	mA
$\frac{\Delta V_o}{\Delta T}$ Output voltage drift	I_o= 5 mA		-0.9			-1			-1.1			-1		mV/°C
e_N output noise voltage	B= 10Hz to 100KHz, T_j= 25°C		250			300			350			400		μV
SVR Supply voltage rejection	f = 120 Hz, ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o} Dropout voltage	T_j= 25°C, I_o= 1A, ΔV_o= 100 mV		1.1			1.1			1.1			1.1		V
I_{sc} Short circuit current			1.3			1.1			0.9			1.1		A
I_{scp} Short circ. peak current	T_j= 25°C		2.2			2.2			2.2			2.2		A

APPLICATION INFORMATION

Fig. 1 - Fixed output regulator



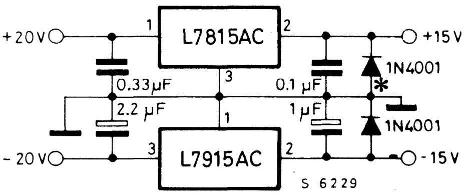
Notes:

(1) To specify an output voltage, substitute voltage value for "XX".

(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.

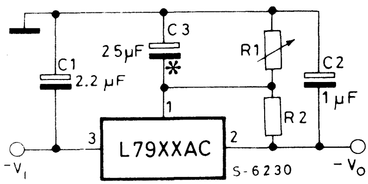
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 - Split power supply (± 15V/1A)



* Against potential latch-up problems.

Fig. 3 - Circuit for increasing output voltage



$$V_O \cong V_{XX} \cdot \frac{R1 + R2}{R2} \qquad \frac{V_{XX}}{R2} > 3\, I_d$$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 - High current negative regulator (-5V/4A with 5A current limiting)

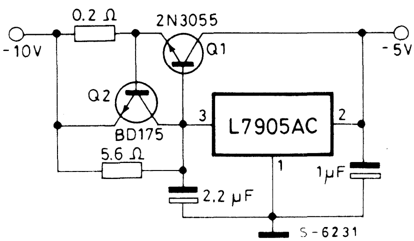
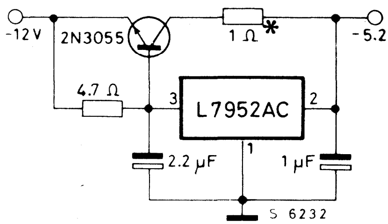


Fig. 5 - Typical ECL system power supply (-5.2V/ 4A)



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

SGS

LM117 LM217 LM317

PRELIMINARY DATA

1.2V to 37V ADJUSTABLE VOLTAGE REGULATOR

The LM 117/LM 217/LM 317 are monolithic integrated circuits in TO-220 and TO-3 packages intended for use as positive adjustable voltage regulator.
They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range.
The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed voltage regulators.
Their main features are:

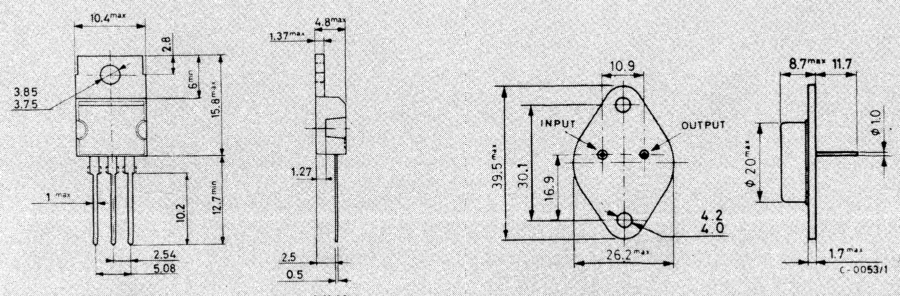
- Output voltage range: 1.2 to 37V
- Output current in excess of 1.5A
- 0.1% line and load regulation
- Floating operation for high voltages
- Complete series of protections: current limiting, thermal shut-down and SOA control.

ABSOLUTE MAXIMUM RATINGS

V_{i-o}	Input-output differential voltage		40	V
I_o	Output current		Internally limited	
T_{op}	Operating junction temperature for:	LM 117	-55 to 150	°C
		LM 217	-25 to 150	°C
		LM 317	0 to 125	°C
P_{tot}	Power dissipation		Internally limited	
T_{stg}	Storage temperature		-65 to 150	°C

MECHANICAL DATA

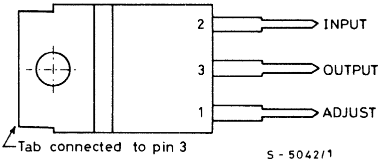
Dimensions in mm

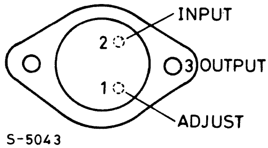


TO-220 TO-3

LM117
LM217
LM317

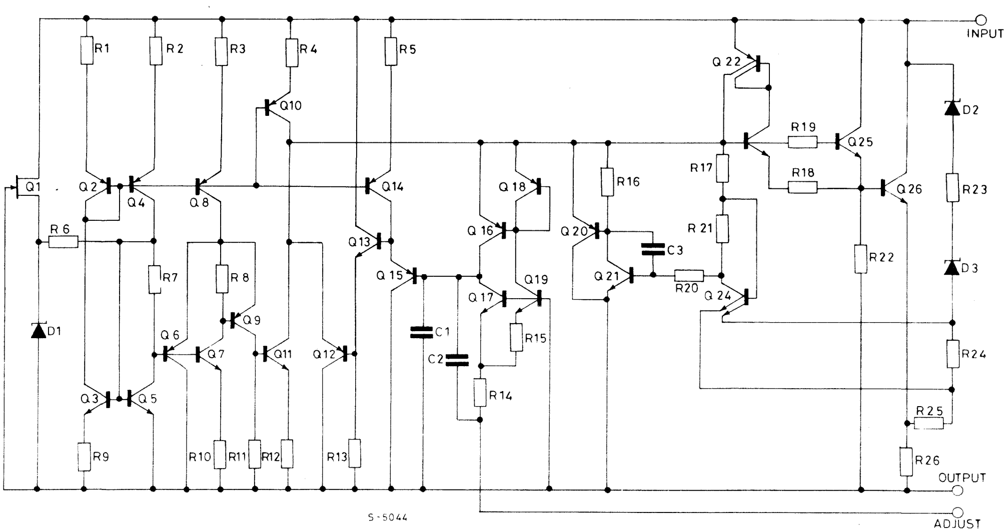
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-220	TO-3
LM 117	—	LM 117K
LM 217	—	LM 217K
LM 317	LM 317T	LM 317K

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (V_i-V_o = 5V, I_o = 500 mA, unless otherwise specified)

Parameter		Test conditions		LM 117/LM 217 Min.	LM 117/LM 217 Typ.	LM 117/LM 217 Max.	LM 317 Min.	LM 317 Typ.	LM 317 Max.	Unit
ΔV_o	Line regulation	V_i-V_o= 3 to 40V	T_j= 25°C		0.01	0.02		0.01	0.04	%/V
					0.02	0.05		0.02	0.07	
ΔV_o	Load regulation	$V_o \leqslant$ 5V I_o= 10mA to 1.5A	T_j= 25°C		5	15		5	25	mV
					20	50		20	70	
		$V_o \geqslant$ 5V I_o= 10 mA to 1.5A	T_j= 25°C		0.1	0.3		0.1	0.5	%
					0.3	1		0.3	1.5	
I_{ADJ}	Adjustment pin current				50	100		50	100	μA
ΔI_{ADJ}	Adjustment pin current	V_i-V_o= 2.5 to 40V I_o= 10 mA to 1.5A			0.2	5		0.2	5	μA
V_{REF}	Reference voltage (between pin 3 and pin 1)	V_i-V_o= 3 to 40V I_o= 10 mA to 1.5A		1.2	1.25	1.3	1.2	1.25	1.3	V
$\frac{\Delta V_o}{V_o}$	Output voltage temperature stability				1			1		%
$I_{o\ min}$	Minimum load current				3.5	5		3.5	10	mA
$I_{o\ max}$	Maximum load current	V_i-$V_o \leqslant$ 15V		1.5	2.2		1.5	2.2		A
		V_i-V_o= 40V			0.4			0.4		
e_N	Output noise (percentage of V_o)	T_j= 25°C, 10Hz to 10KHz			0.003			0.003		%
SVR	Supply voltage rejection (*)	T_j= 25°C f = 120 Hz	C_{ADJ}= 0		65			65		dB
			C_{ADJ}= 10 μF	66	80		66	80		

(*) C_{ADJ} is connected between pin 1 and ground.

Note – Unless otherwise specified the above specs, apply over the following conditions: LM 117 T_j= -55 to 150°C; LM 217 T_j = -25 to 150°C; LM 317 T_j = 0 to 125°C.

Fig. 1 - Output current vs. input-output differential voltage

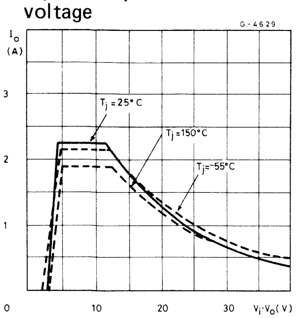


Fig. 2 - Dropout voltage vs. junction temperature

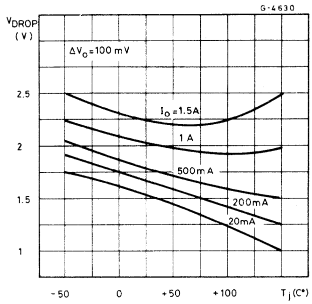
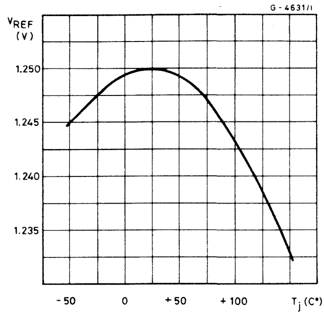


Fig. 3 - Reference voltage vs. junction temperature

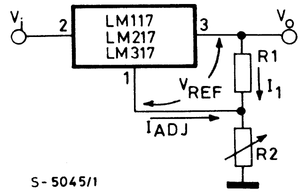


APPLICATION INFORMATION

The LM 117/LM 217/LM 317 provides an internal reference voltage of 1.25V between the output and adjustment terminals. This is used to set a constant current flow across an external resistor divider (see fig. 4), giving an output voltage V_o of:

$$V_o = V_{REF} \left(1 + \frac{R2}{R1}\right) + I_{ADJ}\ R2$$

Fig. 4 - Basic adjustable regulator



The device was designed to minimize the term I_{ADJ} (100 μA max) and to maintain it very constant with line and load changes. Usually, the error term $I_{ADJ} \cdot R2$ can be neglected. To obtain the previous requirement, all the regulator quiescent current is returned to the output terminal, imposing a minimum load current condition. If the load is insufficient, the output voltage will rise.

Since the LM 117/LM 217/LM 317 is a floating regulator and "sees" only the input-to-output differential voltage, supplies of very high voltage with respect to ground can be regulated as long as the maximum input-to-output differential is not exceeded. Furthermore, programmable regulator are easily obtainable and, by connecting a fixed resistor between the adjustment and output, the device can be used as a precision current regulator.

In order to optimise the load regulation, the current set resistor R1 (see fig. 4) should be tied as close as possible to the regulator, while the ground terminal of R2 should be near the ground of the load to provide remote ground sensing.

No external capacitors are required, but performance may be improved with added capacitance as follows:

– An input bypass capacitor of 0.1 μF.

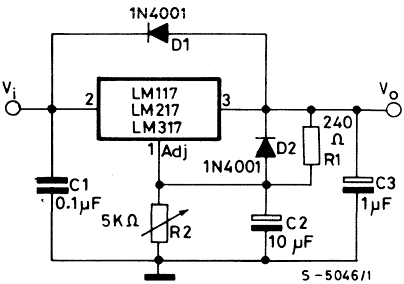
– An adjustment terminal to ground 10 μF capacitor to improve the ripple rejection of about 15 dB (C_{ADJ}).

– An 1 μF tantalum capacitor on the output to improve transient response.

APPLICATION INFORMATION (continued)

In additional to external capacitors, it is good practice to add protection diodes, as shown in fig. 5.

Fig. 5 - Voltage regulator with protection diodes.



D1 protects the device against input short circuit, while D2 protects against output short circuit for capacitors discharging.

Fig. 6 - Slow turn-on 15V regulator

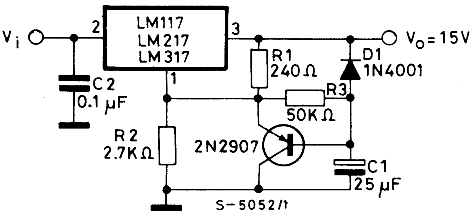
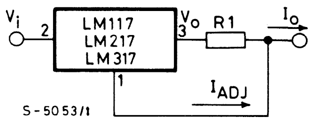


Fig. 7 - Current regulator



$$I_o = \frac{V_{ref}}{R1} + I_{ADJ} \cong \frac{1.25V}{R1}$$

(I_o = 10 mA to 1.5A)

Fig. 8 - 5V electronic shut-down regulator

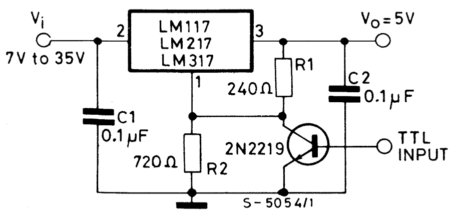
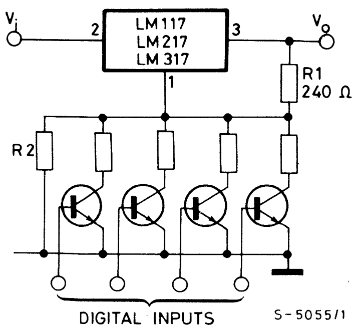


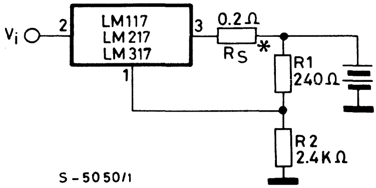
Fig. 9 - Digitally selected outputs



(R2 sets maximum V_o)

APPLICATION INFORMATION (continued)

Fig. 10 - Battery charger (12V).

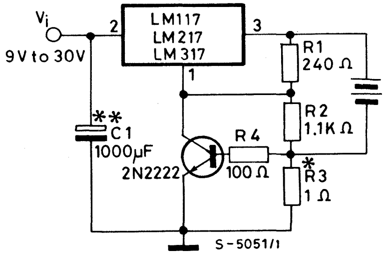


* R_S sets output impedance of charger

$$Z_o = R_s \left(1 + \frac{R2}{R1}\right)$$

Use of R_S allows low charging rates with fully charged battery.

Fig. 11 - Current limited 6V charger.



* R3 sets peak current (0.6A for 1Ω).
** C1 recommended to filter out input transients.

LINEAR INTEGRATED CIRCUITS

SGS **LM 324 LM 324A LM 2902**

LOW POWER QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT POWER SUPPLY
- VERY LOW POWER CONSUMPTION
- INPUT COMMON-MODE RANGE INCLUDING GROUND
- LARGE DC VOLTAGE GAIN (100 dB)

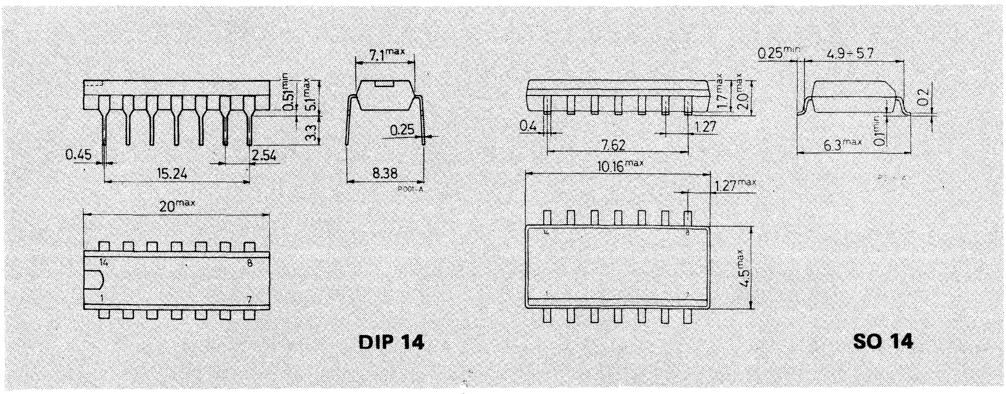
The LM 324 series consists of four indipendent, high gain, internally frequency compensated opamps specifically designed to operate from a single power supply over a wide range of voltages. Both in split and in single supply the current drain is independent of the magnitude of the power supply voltage.
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operating from only a single power supply voltage.
The LM 324 is available in a standard 14-lead dual in-line plastic package and in a 14-lead micropackage version for thick or thin film hybrid circuits.

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage : **LM 324/324A**	32	V
	LM 2902	26	V
V_i	Input voltage (single supply)	-0.3 to 26	V
V_i	Differential input voltage	32	V
P_{tot}	Total power dissipation	400	mW
T_{op}	Operating temperature for : **LM 2902**	-40 to 85	°C
	LM 324/324A	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

MECHANICAL DATA

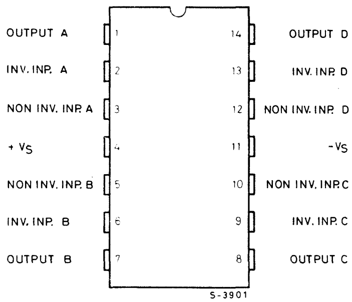
Dimensions in mm



DIP 14 **SO 14**

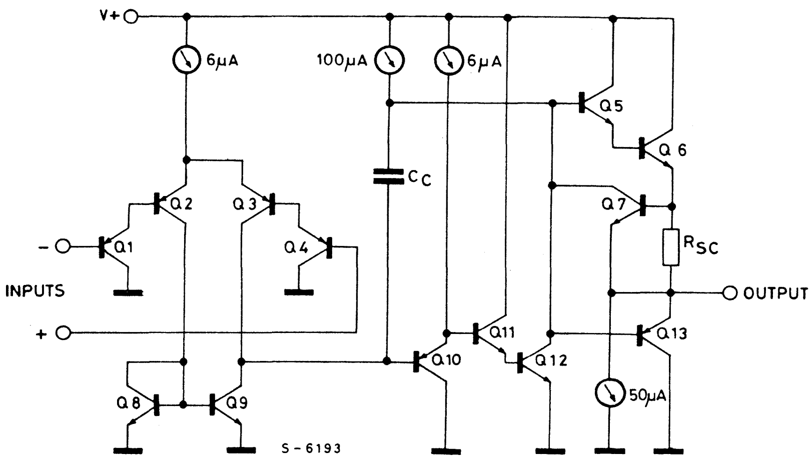
SGS LM324 LM324A LM2902

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	DIP-14	SO-14
LM 324	LM 324N	LM 324CM
LM 324A	LM 324AN	–
LM 2902	LM 2902N	LM 2902CM

SCHEMATIC DIAGRAM
(one section)



THERMAL DATA

			DIP 14	SO 14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200 °C/W	200 °C/W*

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

LM 324
LM 324A
LM 2902

ELECTRICAL CHARACTERISTICS (V_s = +5V, T_{amb} = 0 to 70°C for the LM 324A, LM 324 and T_{amb} = -40 to 85°C for the LM 2902, unless otherwise specified)

Symbol	Parameter	Test conditions		LM 324 Min.	LM 324 Typ.	LM 324 Max.	LM 324A Min.	LM 324A Typ.	LM 324A Max.	LM 2902 Min.	LM 2902 Typ.	LM 2902 Max.	Unit
I_S	Supply current	$R_L = \infty$	V_s = 30V (*)		1.5	3		1.5	3		1.5	3	mA
					0.7	1.2		0.7	1.2		0.7	1.2	
I_b	Input bias current	T_{amb} = 25°C			45	250		45	100		45	250	nA
						500			200			500	
V_{os}	Input offset voltage	R_g = 0, V_s = 5V to 30V (*)	T_{amb} = 25°C		± 2	± 7		± 2	± 3		± 2	± 7	mV
						± 9			± 5			± 10	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 0			7			7	30		7		μV/°C
I_{os}	Input offset current	T_{amb} = 25°C			± 5	± 50		± 5	±30		± 5	± 50	nA
						±150			±75			±200	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	300		10		pA/°C
I_{sc}	Output short circuit to ground current	T_{amb} = 25°C (**)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V, $R_L \geq$ 2 KΩ	T_{amb} = 25°C	88	100		88	100			100		dB
				83			83			83			
	Input common-mode voltage range	V_s = 30V (*)	T_{amb} = 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb} = 25°C	R_L = 2 KΩ			V_s-1.5			V_s-1.5				V
			$R_L \geq$ 10 KΩ									V_s-1.5	
		V_s = 30V (*)	R_L = 2 KΩ	26			26			22			V
			$R_L \geq$ 10 KΩ	27	28		27	28		23	24		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leq$ 10 KΩ			5	20		5	20		5	100	mV
CMR	Common mode rejection	T_{amb} = 25°C		65	70		65	85		50	70		dB
SVR	Supply voltage rejection	T_{amb} = 25°C		65	70		65	100		50	70		dB
CS	Channel separation	f = 1 KHz to 20 KHz, T_{amb} = 25°C (Input referred)			120			120			120		dB
I_o^+	Output source current	V_s = 15V, V_i^+ = 1V, V_i^- = 0V	T_{amb} = 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_o^-	Output sink current	V_i^+ = 0V, V_i^- = 1V, V_o = 200 mV	T_{amb} = 25°C	12	50		12	50					μA
		V_i^- = 1V, V_i^+ = 0V, V_s = 15V	T_{amb} = 25°C	10	20		10	20		10	20		mA
				5	8		5	8		5	8		

(*) V_s = 26V for LM 2902.

(**) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magnitude of V_s. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Fig. 1 - Supply current vs. supply voltage

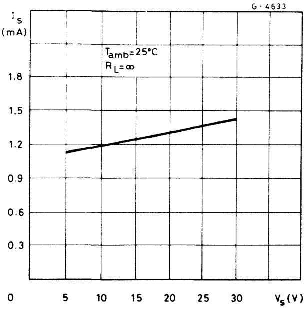


Fig. 2 - Input voltage range vs. supply voltage

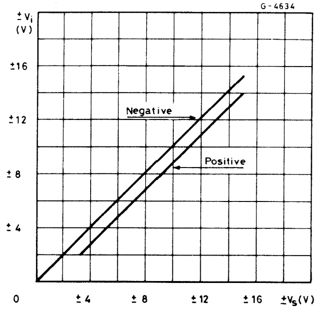


Fig. 3 - Output short circuit current vs. ambient temperature

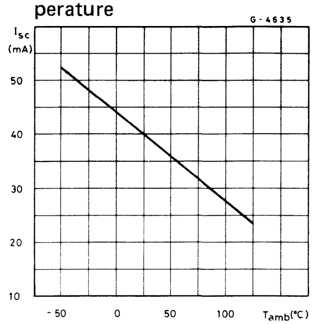


Fig. 4 - Open loop frequency response

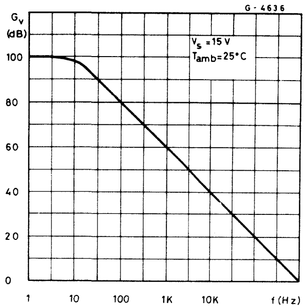


Fig. 5 - Large signal frequency response

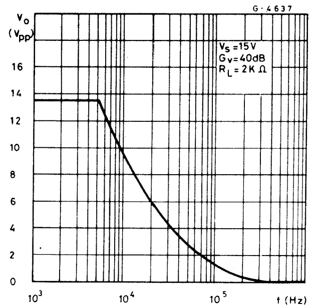
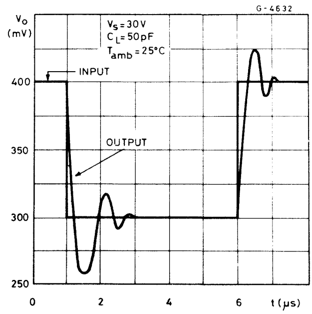


Fig. 6 - Voltage follower pulse response (small signal)



APPLICATION INFORMATION

The LM 324 can operate with a single power supply voltage, has true-differential inputs and remains in the linear mode with an input common-mode voltage of 0V. The four included op amps work over a wide range of power supply voltage with little change in performance characteristics. At 25°C operation is possible down to a minimum supply voltage of 2.3V.

The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_s-1.5V, but either or both inputs can go to +32V without damage.

If the voltage at any of the input leads is driven negative ($V_{in} < -0.3V$), the collector-base junction of the input PNP transitor becomes forward biased and thereby acts as an input diode clamps (max current: 50 mA). In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This can cause the output voltage to go to the positive supply voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns positive ($V_{in} > -0.3V$). The output stage design allows the amplifiers to both source and sink large output currents.

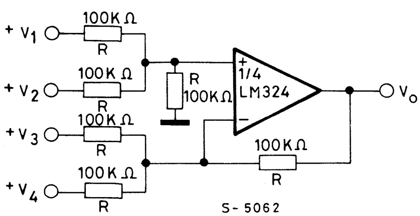
Therefore both NPN and PNP external current boost transistors can be used to extend the power capa-

APPLICATION INFORMATION (continued)

bility of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperature. **Putting direct short-circuits on more than one amplifier at a time, the total IC power dissipation will increase to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers.** The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.
The circuits presented in the following section emphasize operation on a single power supply voltage. If split supplies are used, all the standard op amps configuration can be realised.

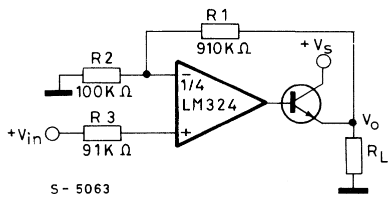
TYPICAL SINGLE SUPPLY APPLICATION CIRCUITS ($V_s = 5V$)

Fig. 7 - DC summing amplifier



where: $V_o = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2)' \geqslant (V_3 + V_4)$ to keep $V_o > 0V$

Fig. 8 - Power amplifier



$V_o = 0V$ for $V_{IN} = 0V$
$G_V = 20$ dB

Fig. 9 - LED driver

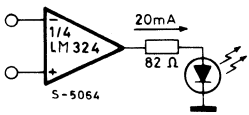


Fig. 10 - Lamp driver

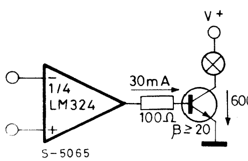
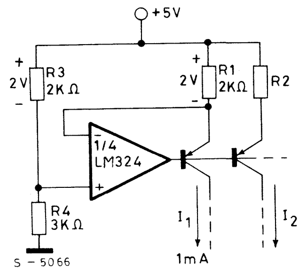


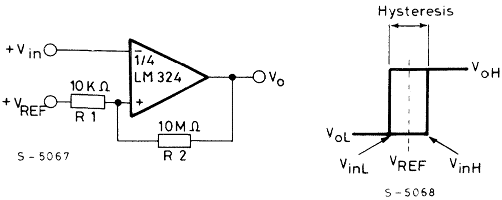
Fig. 11 - Fixed current sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

TYPICAL SINGLE SUPPLY APPLICATION CIRCUITS (continued)

Fig. 12 - Comparator with Hysteresis

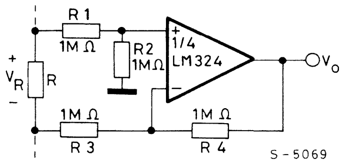


$$V_{in\,L} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Fig. 13 - Ground referencing a differential input signal



$$V_O = V_R$$

Fig. 14 - Driving TTL

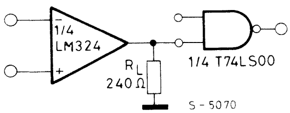


Fig. 15 - Squarewave oscillator

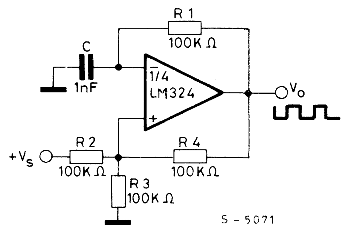
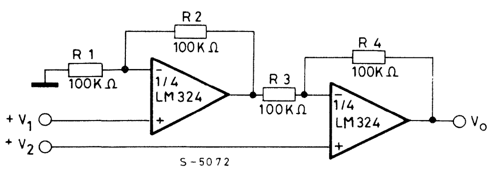


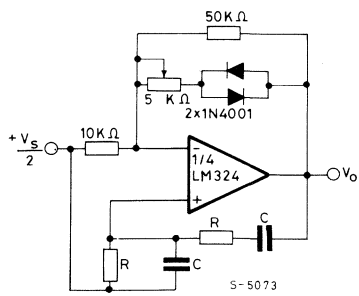
Fig. 16 - High input Z, DC differential amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V2 - V1)$$

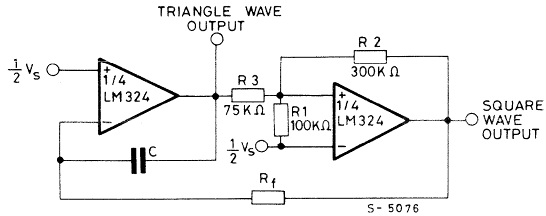
Fig. 17 - Wien bridge oscillator



$$f_o = \frac{1}{2\pi RC}$$

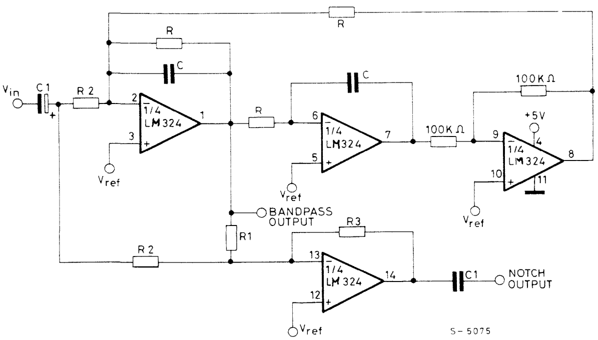
TYPICAL SINGLE SUPPLY APPLICATION CIRCUITS (continued)

Fig. 18 - Function generator



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \qquad R3 = \frac{R2\ R1}{R2 + R1}$$

Fig. 19 - Bi-Quad filter



$f_o = \frac{1}{2\pi\ RC}$; R1= QR; R2= $\frac{R1}{G_{BP}}$;

$V_{ref} = \frac{1}{2}\ V_s$; R3= G_N R2; C1= 10C

Example:

f_o = 1 KHz	R = 160 KΩ
Q = 10	C = 1 nF
G_{BP}= 1	R1= 1.6 MΩ
G_N= 1	R2= 1.6 MΩ
	R3= 1.6 MΩ

Where: G_{BP}= Center Frequency Gain
G_N = Passband Notch Gain

LM339
LM339A
LM2901

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

QUAD VOLTAGE COMPARATOR

- SINGLE SUPPLY OPERATION +2.0V to +36V
- DUAL SUPPLY OPERATION ±1.0V to ±18V
- ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL
- LOW CURRENT DRAIN 800μA TYP
- COMPATIBLE WITH ALL FORMS OF LOGIC
- LOW INPUT BIAS CURRENT 25nA TYP
- LOW INPUT OFFSET CURRENT ±5nA TYP
- LOW OFFSET VOLTAGE ±2mV

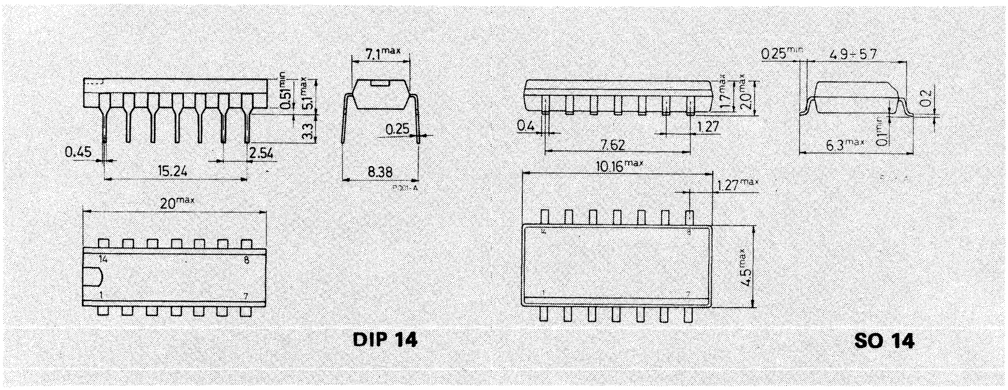
The LM339, LM339A and LM2901 are monolithic integrated circuits in a 14-lead dual in-line plastic package and in a 14-lead micropackage. They consists of four independent precision voltage comparators and are specially designed to offer a versatility as high as possible; application areas include limit comparators, A/D converters, waveforms generators, high voltage logic gates and so on. Furthermore, the open collector output stage provides easy interfacing with all types of logic circuitry.

ABSOLUTE MAXIMUM RATINGS

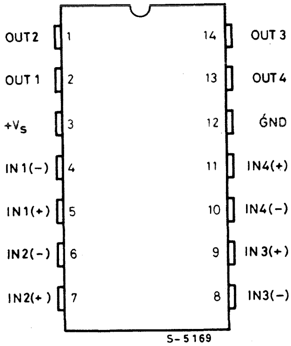
V_s	Supply voltage	±18 or +36	V
V_I	Input voltage range	-0.3 to 36	V
V_i	Differential input voltage	36	V
I_i	Input current ($V_{in} < -0.3\ V_{dc}$)	50	mA
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	600	mW
T_{op}	Operating temperature LM339/339A	0 to 70	°C
	LM2901	-40 to 85	°C
T_{stg}	Storage and junction temperature	-65 to 150	°C

MECHANICAL DATA

Dimensions in mm

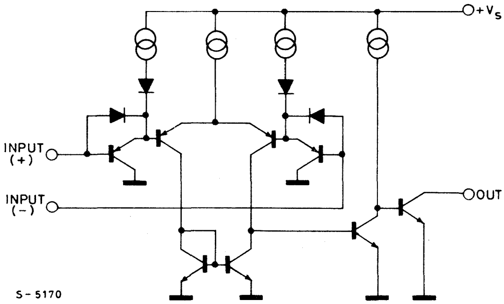


CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	DIP-14	SO-14
LM339 LM339A	LM339N LM339AN	LM339CM —
LM2901	LM2901N	LM2901CM

SCHEMATIC DIAGRAM
(each section)



THERMAL DATA

			DIP-14	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200 °C/W	200 °C/W*

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

LM339
LM339A
LM2901

ELECTRICAL CHARACTERISTICS (V_s = +5V; T_{amb} = 25°C, unless otherwise specified)

	Parameter	Test conditions		LM339A Min.	LM339A Typ.	LM339A Max.	L339 Min.	L339 Typ.	L339 Max.	LM2901 Min.	LM2901 Typ.	LM2901 Max.	Unit
V_{os}	Input offset voltage	At out. switch point $V_o \cong 1.4V$; $R_g = 0$			±1	±2		±2	±5		±2	±7	mV
		V_{REF} = 1.4V	$T_{low} \leq T_{amb} \leq T_{high}$			±4			±9		±9	±15	
I_b	Input bias current (1)	Output in linear range			25	250		25	250		25	250	nA
			$T_{low} \leq T_{amb} \leq T_{high}$			400			400		200	500	
I_{os}	Input offset current				±5	±50		±5	±50		±5	±50	nA
			$T_{low} \leq T_{amb} \leq T_{high}$			±150			±150		±50	±200	
	Input Common-Mode voltage range (2)			0		V_s-1,5	0		V_s-1,5	0		V_s-1,5	V
			$T_{low} \leq T_{amb} \leq T_{high}$	0		V_s-2	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.8	2		0.8	2		0.8	2	mA
I_s	Supply current	V_s = 30V $R_L = \infty$										2.5	mA
G_V	Voltage gain	$R_L \geq 15$ KΩ, V_s = 15V		94	106			106		88	106		dB
	Large signal response time	V_{IN} = TTL logic swing; V_{REF} = +1.4V; R_L = 5.1KΩ V_{RL} = 5V			300			300			300		ns
T_r	Response time (3)	V_{RL} = 5V;	R_L = 5.1V		1.3			1.3			1.3		µs
I_o	Output sink current	$V_{IN(-)} \geq 1V$; $V_o \leq 1.5V$	$V_{IN(+)}$ = 0V;	6	16		6	16		6	16		mA
V_{sat}	Output saturation	$V_{IN(-)} \geq 1V$ $V_{IN(+)}$ = 0V $I_{sink} \leq 4mA$			150	400		150	400			400	mV
			$T_{low} \leq T_{amb} \leq T_{high}$			700			700		200	700	
$I_{o\ leak}$	Output leakage	$V_{IN(+)} \geq 1V$ $V_{IN(-)}$ = 0V	V_o = 5V		0.1			0.1			0.1		nA
			$T_{low} \leq T_{amb} \leq T_{high}$ V_o = 30V			1			1			1	µA
V_{ID}	Differential input voltage	All $V_{IN} \geq 0V$ (or $-V_s$ if split supply is used);	$T_{low} \leq T_{amb} \leq T_{high}$			$+V_s$			$+V_s$			$+V_s$	V

LM 2901 — T_{low} = -40°C, T_{high} = +85°C
LM339/339A — T_{low} = 0°C, T_{high} = +70°C

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

TYPICAL CHARACTERISTICS (LM339 – LM339A)

Fig. 1 - Supply current vs. supply voltage

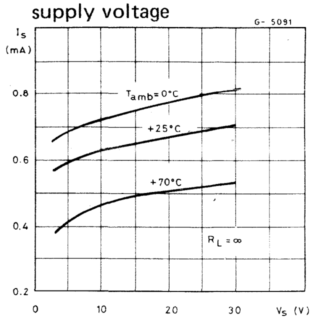


Fig. 2 - Input current vs. supply voltage

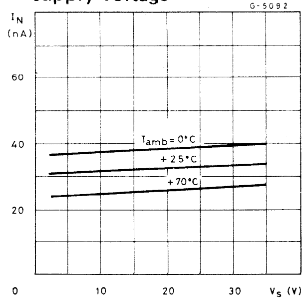


Fig. 3 - Output saturation voltage

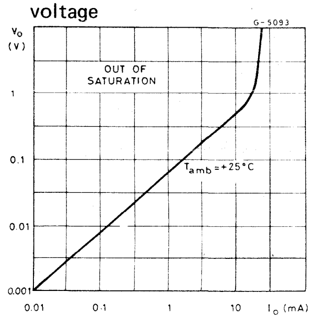


Fig. 4 - Response time

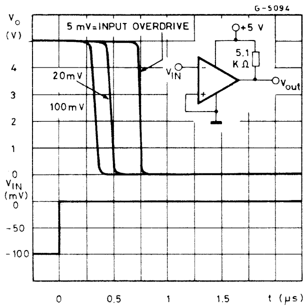
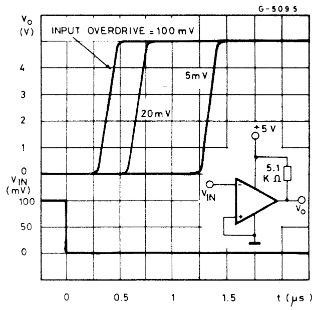


Fig. 5 - Response time



TYPICAL CHARACTERISTICS (LM2901)

Fig. 6 - Supply current vs. supply voltage

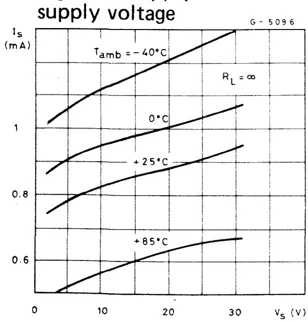


Fig. 7 - Input current vs. supply voltage

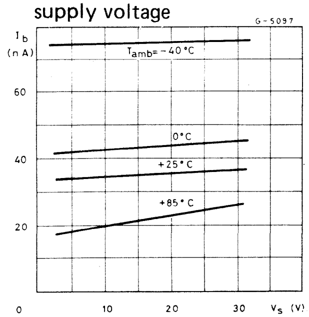
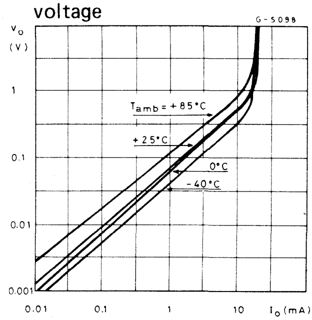


Fig. 8 - Output saturation voltage



APPLICATION INFORMATION

The LM 339 includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.
To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.
It is good design practice to ground all unused pins.
The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

The output of the LM 339 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.
The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Fig. 9 - Basic comparator

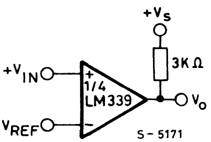


Fig.10- Non-inverting comparator with Hysteresis

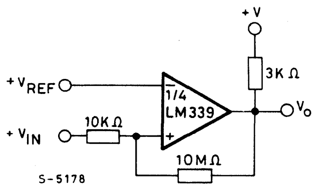


Fig.11- Inverting comparator with Hysteresis

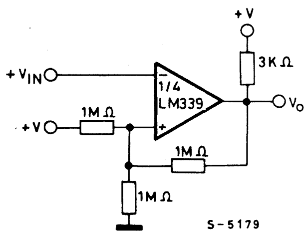


Fig.12- Driving C/MOS

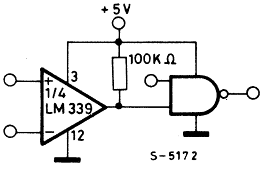
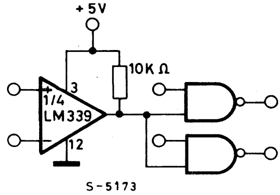


Fig.13- Driving TTL



APPLICATION INFORMATION (continued)

Fig.14- AND gate

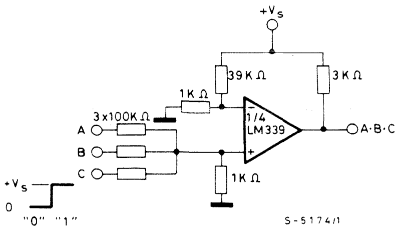


Fig.15- OR gate

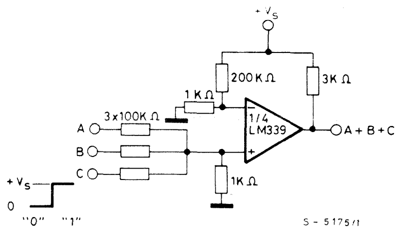


Fig.16- Large fan-in AND gate

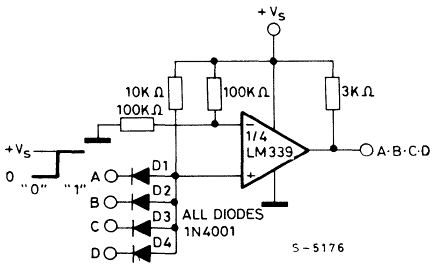


Fig.17- Squarewave oscillator

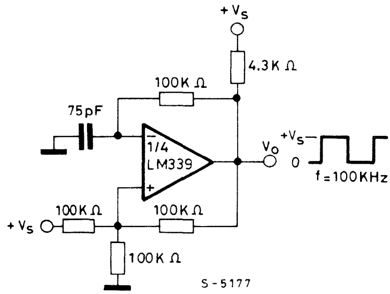


Fig. 18 - Time delay generator

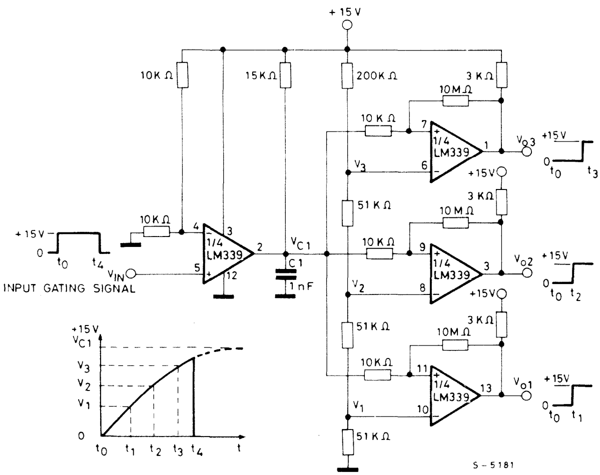
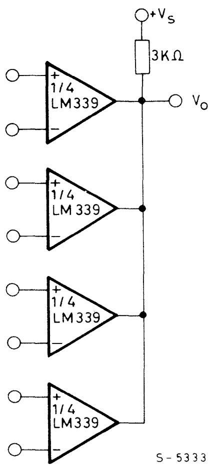


Fig. 19 - ORing the outputs



APPLICATION INFORMATION (continued)

Fig. 20 - Peak audio level display

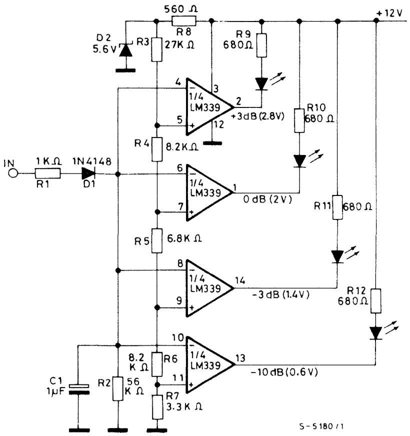


Fig. 21 - PC Board and component layout of the circuit of fig. 12

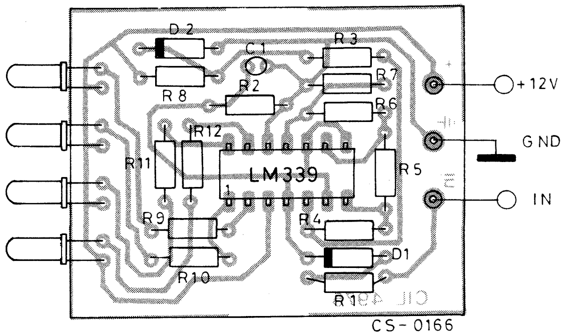
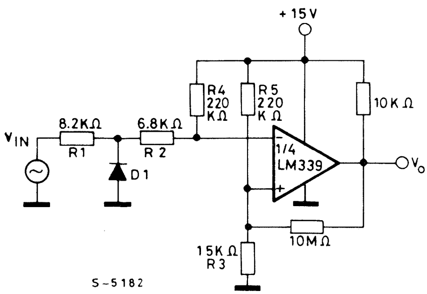


Fig. 22 - Zero crossing detector (single supply)



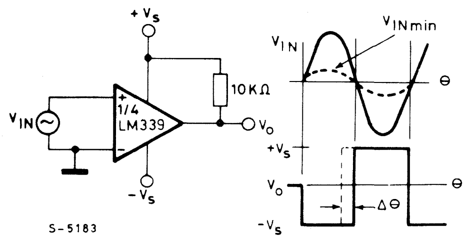
D1 prevents input from going negative by more than 0.6V:

$$R1 + R2 = R3$$

$$R3 \leqslant \frac{R5}{10}$$ for smaller error in zero crossing

Fig. 23 - Zero crossing detector (split supplies)

$V_{INmin} \approx 0.4V$ peak for 1% phase distortion ($\Delta\ \theta$)



DUAL OPERATIONAL AMPLIFIER

- SINGLE SUPPLY (3V to 30V)
  OR DUAL SUPPLIES (± 1.5V to ± 15V)
- VERY LOW SUPPLY CURRENT DRAIN (500 μA) ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIASING CURRENT (45 nA TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE (2 mV) and OFFSET CURRENT (5 nA)
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN

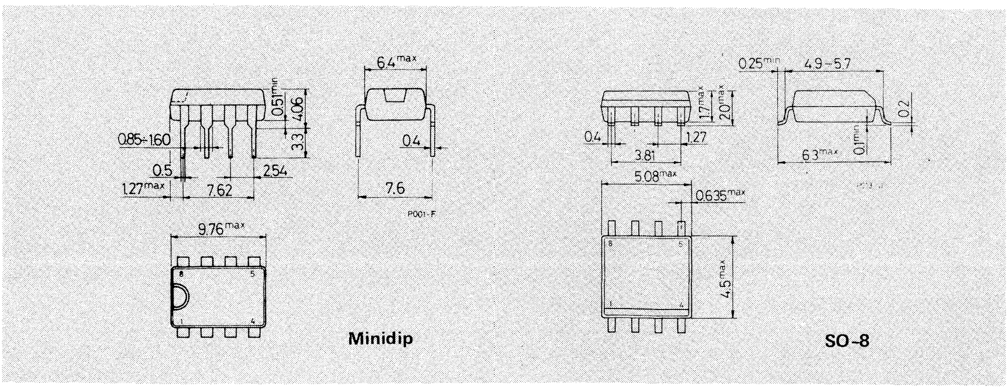
The LM358 series consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the supply voltage.
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated. The LM358 is available in minidip package and in a 8-lead micropackage version.

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage: **LM358/358A**	32 or ±16	V
	LM2904	26 or ±13	V
V_i	Differential input voltage	32	V
V_i	Input voltage	-0.3 to +32	V
P_{tot}	Power dissipation	665	mW
	Output short-circuit to GND $V+ < 15V$ and $T_{amb} = 25°C$	Continuous	
T_{op}	Operating temperature : **LM358/358A**	0 to 70	°C
	LM2904	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

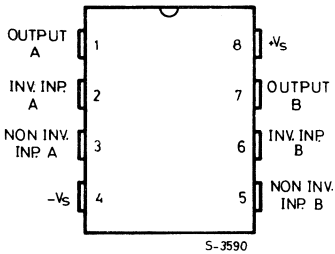
MECHANICAL DATA

Dimensions in mm



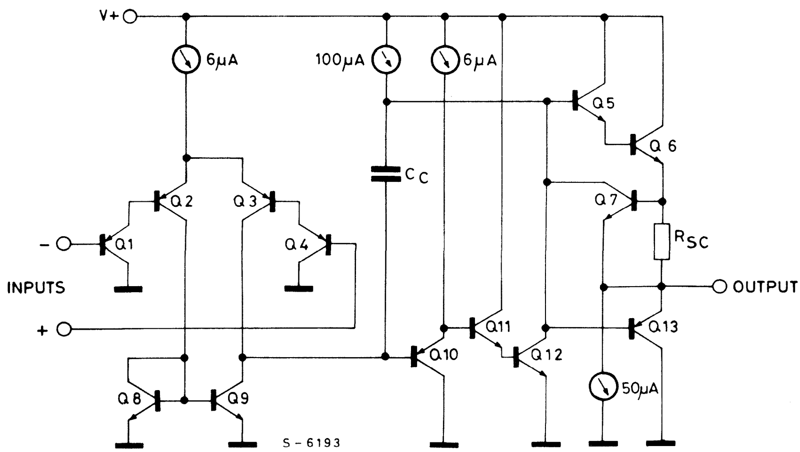
LM358 LM358A LM2904

CONNECTION AND ORDERING NUMBER
(top view)



TYPE	MINIDIP	SO-8
LM358	LM358N	LM358CM
LM358A	LM358AN	–
LM2904	LM2904N	LM2904CM

SCHEMATIC DIAGRAM (One section only)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max. 120 °C/W

ELECTRICAL CHARACTERISTICS (V_s = 5V, T_{amb}= 0 to 70°C for the LM358, LM358 and T_{amb}= -40 to 85°C for the LM2904, unless otherwise specified)

	Parameter	Test conditions		LM 358 Min.	LM 358 Typ.	LM 358 Max.	LM 358A Min.	LM 358A Typ.	LM 358A Max.	LM 2904 Min.	LM 2904 Typ.	LM 2904 Max.	Unit
I_S	Supply current	$R_L = \infty$	V_s = 30V (*)		1	2		11	2		1	2	mA
					0.5	1.2		0.5	1.2		0.5	1.2	
I_b	Input bias current	T_{amb}= 25°C			45	250		45	100		45	250	nA
						500			200			500	
V_{os}	Input offset voltage	R_g= 0, V_s = 5V to 30V (*)	T_{amb}= 25°C		± 2	± 7		± 2	± 3		± 2	± 7	mV
						± 9			± 5			± 10	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g= 0			7			7	30		7		μV/°C
I_{os}	Input offset current	T_{amb}= 25°C			± 5	± 50		± 5	±30		± 5	± 50	nA
						±150			±75			±200	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	300		10		pA/°C
I_{sc}	Output short circuit to ground current	T_{amb}= 25°C (**)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V, $R_L \geq$ 2 KΩ	T_{amb}= 25°C	88	100		88	100			100		dB
				83			83			83			
	Input common-mode voltage range	V_s = 30V (*)	T_{amb}= 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb}= 25°C	R_L= 2 KΩ			V_s-1.5			V_s-1.5				V
			$R_L \geq$ 10 KΩ									V_s-1.5	
		V_s = 30V (*)	R_L= 2 KΩ	26			26			22			V
			$R_L \geq$ 10 KΩ	27	28		27	28		23	24		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leq$ 10 KΩ			5	20		5	20		5	100	mV
CMR	Common mode rejection	T_{amb}= 25°C		65	70		65	85		50	70		dB
SVR	Supply voltage rejection	T_{amb}= 25°C		65	70		65	100		50	70		dB
CS	Channel separation	f = 1 KHz to 20 KHz, T_{amb}= 25°C (Input referred)			120			120			120		dB
I_o^+	Output source current	V_s = 15V, V_{i^+} = 1V, V_{i^-} = 0V	T_{amb}= 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_o^-	Output sink current	V_{i^+} = 0V, V_{i^-} = 1V, V_o= 200 mV	T_{amb}= 25°C	12	50		12	50					μA
		V_{i^-} = 1V, V_{i^+} = 0V, V_s= 15V	T_{amb}= 25°C	10	20		10	20		10	20		mA
				5	8		5	8		5	8		

(*) 26V for LM2904.

(**) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magnitude of V_S. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Fig. 1 - Supply current

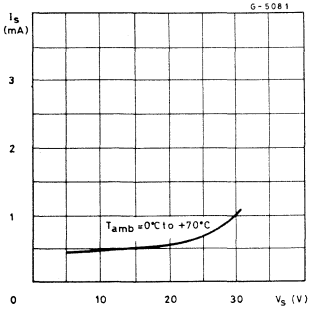


Fig. 2 - Voltage gain

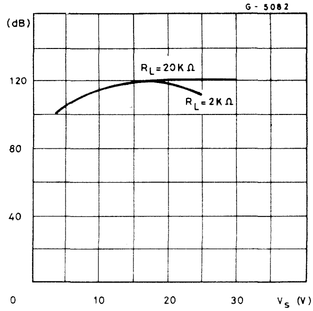


Fig. 3 - Open loop frequency response

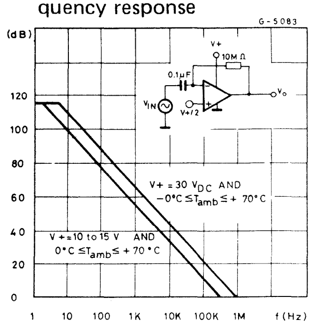


Fig. 4 - Large signal frequency response

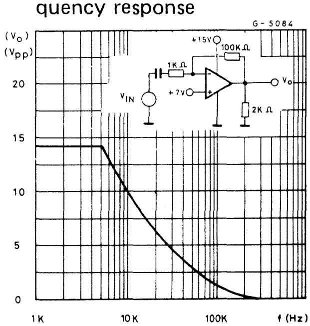


Fig. 5 - Output characteristics (current sourcing)

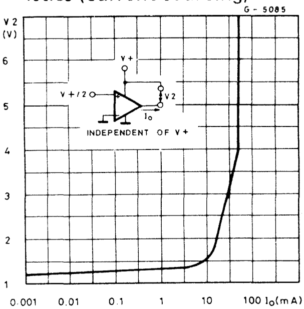


Fig. 6 - Output characteristics (current sinking)

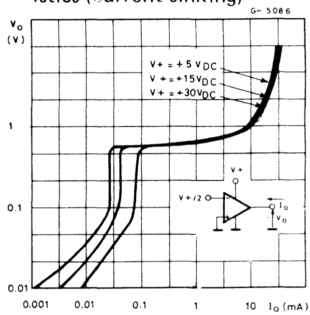


Fig. 7 - Input voltage range

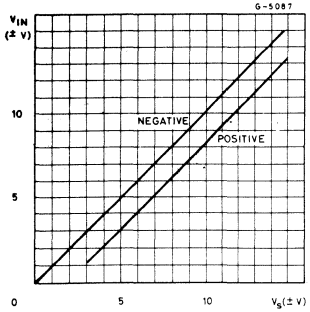


Fig. 8 - Input current

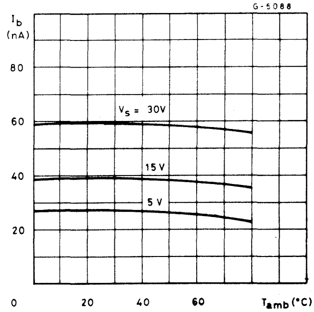
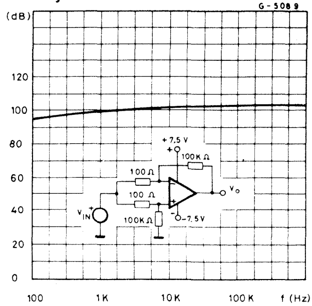


Fig. 9 - Common mode rejection ratio



APPLICATION INFORMATION

Fig. 10 - Full wave rectifier

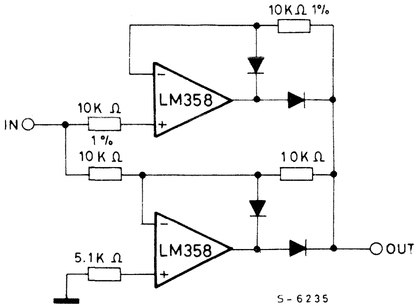


Fig. 11 - Half wave rectifier

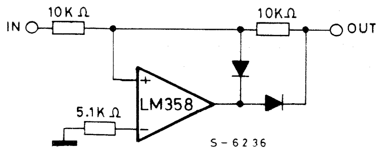
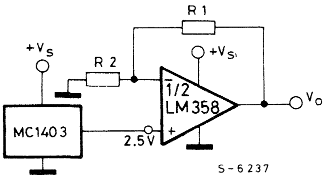
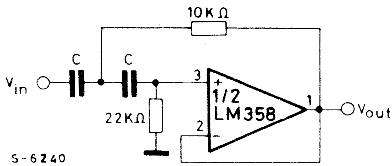


Fig. 12 - Voltage reference



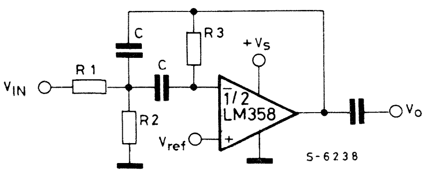
$$V_o = 2.5\ V\ \left(1 + \frac{R1}{R2}\right)$$

Fig. 14 - High-pass filter



f_c = 100 Hz with C = 0.1 μF

Fig. 13 - Multiple feedback bandpass filter



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

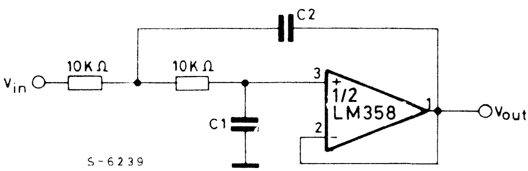
$$R3 = \frac{Q}{\pi f_o C}\ ;\ R1 = \frac{R3}{2A(f_o)}\ ;\ R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier

$\frac{Q_o\ f_o}{BW} < 0.1$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Fig. 15 - Low-pass filter



f_c = 3KHz with C1 = 3.9 nF
and C2 = 6.8 nF.

SGS

LM393
LM393A
LM2903

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

DUAL VOLTAGE COMPARATOR

- SINGLE SUPPLY OPERATION +2.0V to + 36V
- DUAL SUPPLY OPERATION ±1.0V to ±18V
- ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL
- LOW CURRENT DRAIN 400μA TYP
- COMPATIBLE WITH ALL FORMS OF LOGIC
- LOW INPUT BIAS CURRENT 25nA TYP
- LOW INPUT OFFSET CURRENT ±5nA TYP
- LOW OFFSET VOLTAGE ±2mV

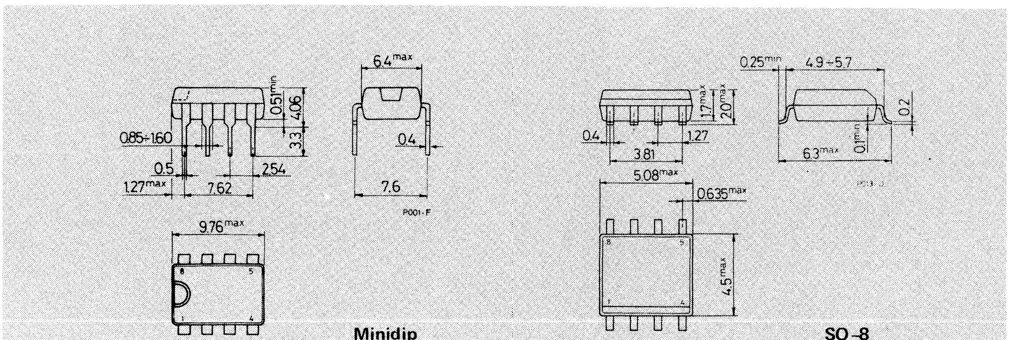
The LM393, LM393A and LM2903 are monolithic integrated circuits in Minidip package and in a 8-lead micropackage. They consists of two independent precision voltage comparators and are specially designed to offer a versatility as high as possible; application areas include limit comparators, A/D converters, waveforms generators, high voltage logic gates and so on. Furthermore, the open collector output stage provides easy interfacing with all types of logic circuitry.

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	±18 or +36	V
V_I	Input voltage range	-0.3 to 36	V
V_i	Differential input voltage	36	V
I_i	Input current ($V_{in} < -0.3\ V_{dc}$)	50	mA
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	600	mW
T_{op}	Operating temperature LM393/393A	0 to 70	°C
	LM2903	-40 to 85	°C
T_{stg}	Storage and junction temperature	-65 to 150	°C

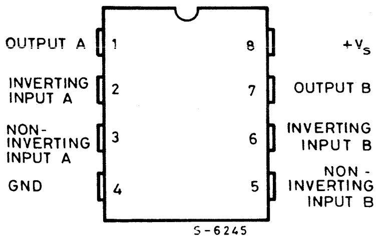
MECHANICAL DATA

Dimensions in mm



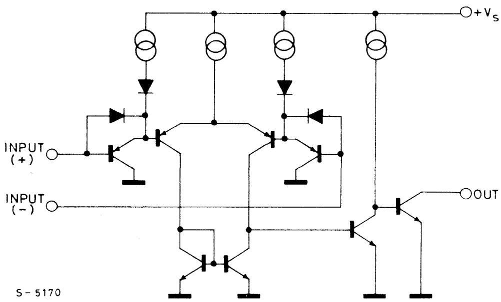
Minidip SO-8

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	MINIDIP	SO-8
LM393 LM393A	LM393N LM393AN	LM393CM –
LM2903	LM2903N	LM2903CM

SCHEMATIC DIAGRAM
(each section)



THERMAL DATA

			MINIDIP	SO-8
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max.	200°C/W	200°C/W*

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = +5V; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		LM393A			LM393			LM2903			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out. switch point $V_o \cong 1.4V$; $R_g = 0$			±1	±2		±2	±5		±2	±7	mV
		V_{REF} = 1.4V	$T_{low} \leq T_{amb} \leq T_{high}$			±4			±9		±9	±15	
I_b	Input bias current (1)	Output in linear range			25	250		25	250		25	250	nA
			$T_{low} \leq T_{amb} \leq T_{high}$			400			400		200	500	
I_{os}	Input offset current				±5	±50		±5	±50		±5	±50	nA
			$T_{low} \leq T_{amb} \leq T_{high}$			±150			±150		±50	±200	
	Input Common-Mode voltage range (2)			0		V_s-1,5	0		V_s-1,5	0		V_s-1,5	V
			$T_{low} \leq T_{amb} \leq T_{high}$	0		V_s-2	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.4	1		0.4	1		0.4	1	mA
I_s	Supply current	V_s = 30V $R_L = \infty$				2.5			2.5			2.5	mA
G_v	Voltage gain	$R_L \geq 15\ K\Omega$, V_s = 15V		94	106			106		88	106		dB
	Large signal response time	V_{IN} = TTL logic swing; V_{REF} = +1.4V; R_L = 5.1KΩ V_{RL} = 5V			300			300			300		ns
T_r	Response time (3)	V_{RL} = 5V;	R_L = 5.1V		1.3			1.3			1.3		µs
I_o	Output sink current	$V_{IN(-)} \geq 1V$; $V_o \leq 1.5V$	$V_{IN(+)}$ = 0V;	6	16		6	16		6	16		mA
V_{sat}	Output saturation	$V_{IN(-)} \geq 1V$ $V_{IN(+)}$ = 0V $I_{sink} \leq 4mA$			150	400		150	400			400	mV
			$T_{low} \leq T_{amb} \leq T_{high}$			700			700		200	700	
$I_{o\ leak}$	Output leakage	$V_{IN(+)} \geq 1V$ $V_{IN(-)}$ = 0V	V_o = 5V		0.1			0.1			0.1		nA
			$T_{low} \leq T_{amb} \leq T_{high}$ V_o = 30V			1			1			1	µA
V_{ID}	Differential input voltage	All $V_{IN} \geq$ 0V (or $-V_s$ if split supply is used);	$T_{low} \leq T_{amb} \leq T_{high}$			$+V_s$			$+V_s$			$+V_s$	V

LM2903 $-T_{low}$ = -40°C, T_{high} = +85°C

LM393/393A $-T_{low}$ = 0°C, T_{high} = +70°C

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

APPLICATION INFORMATION

The LM393 includes two high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.
To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.
It is good design practice to ground all unused pins.
The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than --0.3V should not be used: an input clamping diode can be used as protection.

The output of the LM393 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.
The output sink current capability is approximately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Fig. 1 - Basic comparator

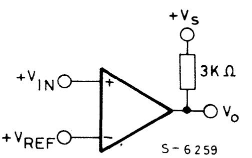


Fig. 2 - Non-inverting comparator with Hysteresis

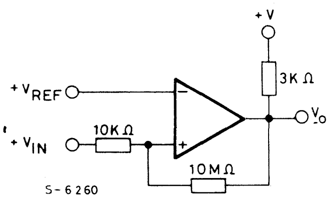


Fig. 3 - Inverting comparator with Hysteresis

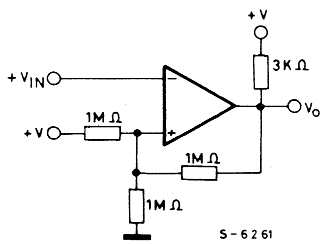


Fig. 4 - Driving C/MOS

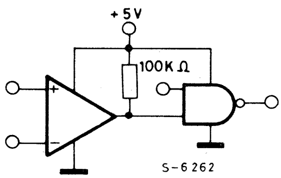
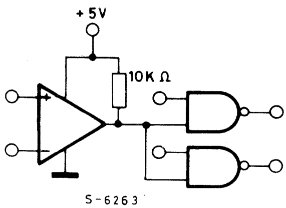


Fig. 5 - Driving TTL



APPLICATION INFORMATION (continued)

Fig. 6 - AND gate

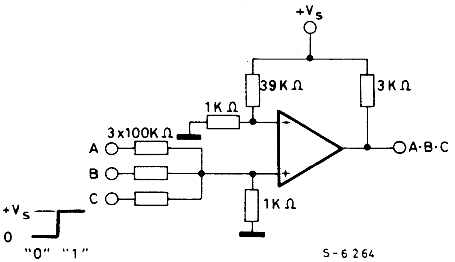


Fig. 7 - OR gate

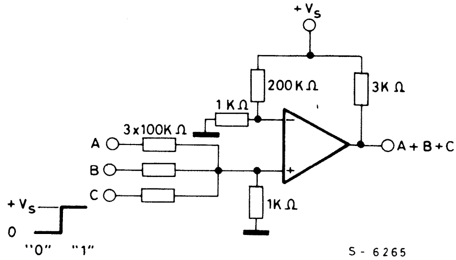


Fig. 8 - Large fan-in AND gate

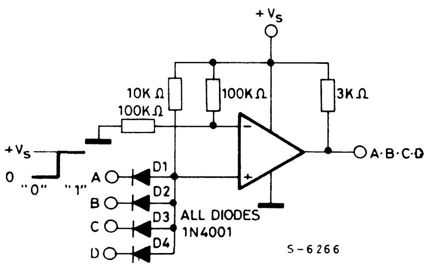


Fig. 9 - Squarewave oscillator

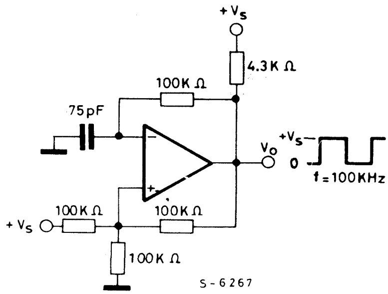


Fig. 10 - Pulse generator

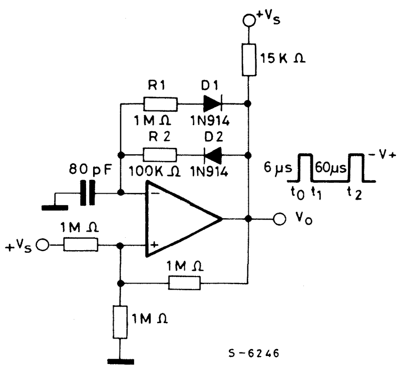
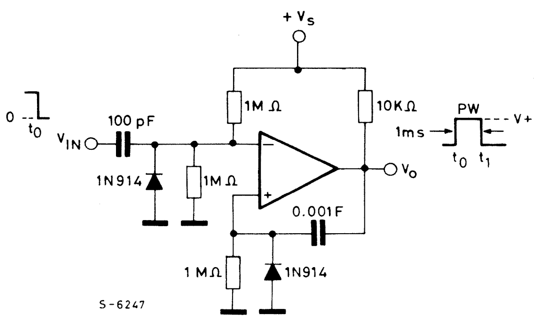


Fig. 11 - One-shot multivibrator



LINEAR INTEGRATED CIRCUITS

SGS **LM723 LM723C**

HIGH PRECISION VOLTAGE REGULATOR

- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING

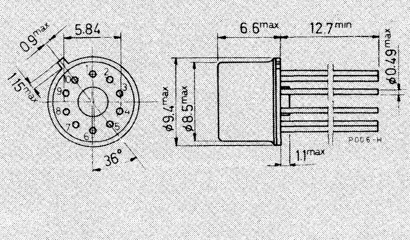
The LM723 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic package and 10-lead Metal Can (TO-100 type). The circuit provides internal current limiting. When the output current excedes 150 mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

ABSOLUTE MAXIMUM RATINGS

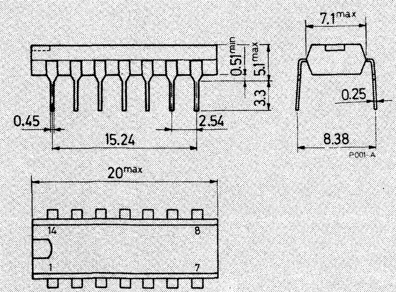
		LM723	LM723C
V_i	Input voltage	40 V	40 V
ΔV_{i-o}	Dropout voltage	40 V	40 V
I_o	Output current	150 mA	150 mA
I_{ref}	Current from V_{ref}	15 mA	25 mA
P_{tot}	Power dissipation (at T_{amb} = 70°C) Plastic DIP	—	1 W
	TO-100	520 mW	520 mW
T_{op}	Operating junction temperature	-25 to 150 °C	0 to 70 °C
T_{stg}	Storage temperature	-65 to 150 °C	-65 to 150 °C

MECHANICAL DATA

Dimensions in mm



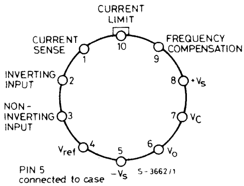
TO-100

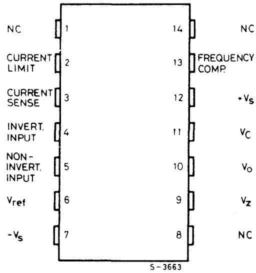


DIP

LM723
LM723C

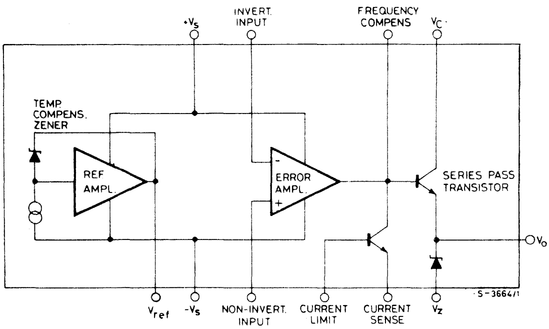
CONNECTION DIAGRAM AND ORDERING NUMBERS
(top views)



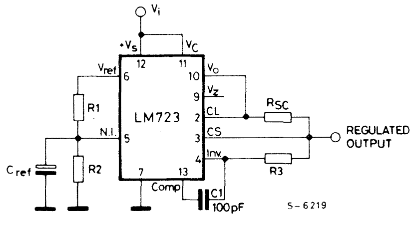


Type	TO-100	Plastic DIP
LM 723	LM 723H	–
LM 723C	LM 723 CH	LM 723 CN

BLOCK DIAGRAM



TEST CIRCUIT
(Pin configuration relative to the Plastic packag



$V_i = 12V$
$V_o = 5V$
$I_o = 1$ mA
$R_1//R_2 \leq 10$ KΩ

THERMAL DATA

			TO-100	Plastic DIP
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	80 °C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	LM 723C Min.	LM 723C Typ.	LM 723C Max.	LM 723 Min.	LM 723 Typ.	LM 723 Max.	Unit
$\frac{\Delta V_o}{\Delta V_i}$	Line regulation	V_i = 12 to 15V V_i = 12 to 40V		0.01 0.1	0.1 0.5		0.01 0.02	0.1 0.2	%
		V_i = 12 to 15V; $T_{min} \leq T_{amb} \leq T_{max}$			0.3			0.3	%
$\frac{\Delta V_o}{V_o}$	Load regulation	I_o = 1 to 50 mA		0.03	0.2		0.03	0.15	%
		$T_{min} \leq T_{amb} \leq T_{max}$ I_o = 1 to 10 mA			0.6			0.6	%
V_{ref}	Reference voltage	I_{ref}= 160 μA	6.8	7.15	7.5	6.95	7.15	7.35	V
SVR	Ripple rejection	f = 100 Hz to 10 KHz C_{ref}= 0 C_{ref}= 5 μF		74 86			74 86		dB dB
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				150			150	$\frac{ppm}{°C}$
I_{sc}	Short circuit current limiting	R_{sc}= 10Ω V_o= 0		65			65		mA
V_i	Input voltage range		9.5		40	9.5		40	V
V_o	Output voltage range		2		37	2		37	V
V_i-V_o			3		38	3		38	V
I_d	Quiescent drain current	I_o = 0 V_i = 30V		2.3	4		2.3	5	mA
	Long term stability			0.1			0.1		$\frac{\%}{1000\ hrs}$
e_N	Output noise voltage	BW= 100 Hz to 10 KHz C_{ref}= 0 C_{ref}= 5 μF		20 2.5			20 2.5		μV μV
V_z	Output zener voltage (for plastic package only)	I_z = 1 mA	6.9		7.7				V

Note: T_{min} = 0°C (LM723C); -25°C (LM723).
T_{max}= 70°C (LM723C); 150°C (LM723).

Fig. 1 - Maximum output current vs. voltage drop

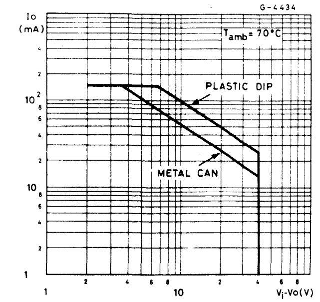


Fig. 2 - Current limiting characteristics

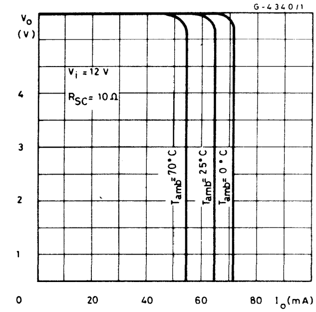


Fig. 3 - Current limiting characteristics vs. junction temperature

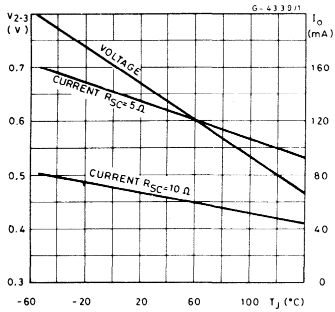


Fig. 4 - Load regulation characteristics without current limiting

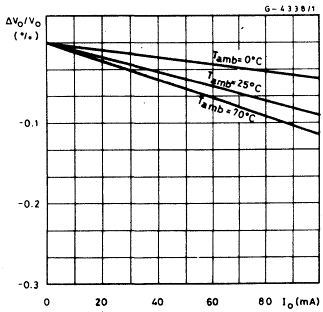


Fig. 5 - Load regulation characteristics with current limiting

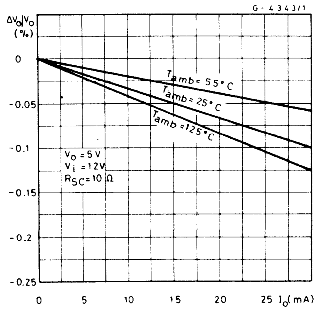


Fig. 6 - Load regulation characteristics with current limiting

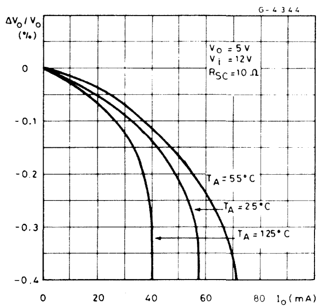


Fig. 7 - Line regulation vs. voltage drop

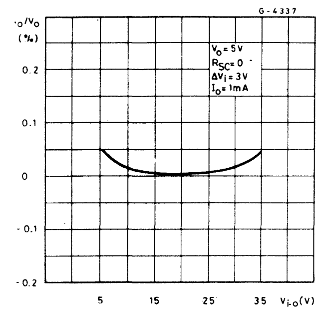


Fig. 8 - Load regulation vs. voltage drop

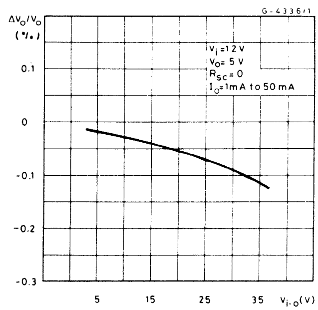


Fig. 9 - Quiescent drain current vs. input voltage

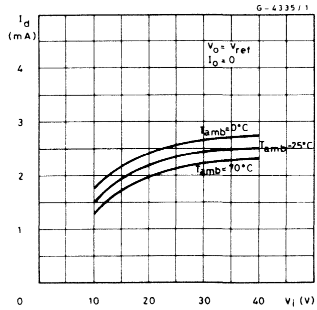


Fig. 10 - Line transient response

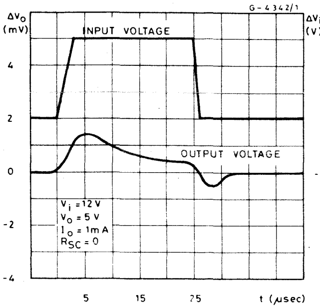


Fig. 11 - Load transient response

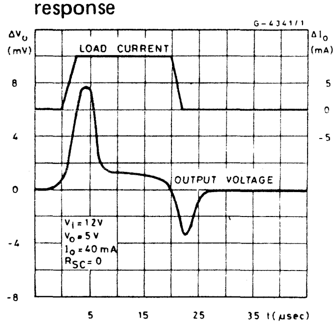


Fig. 12 - Output impedance vs. frequency

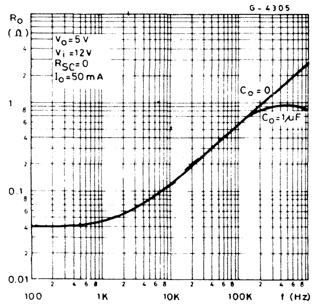


Table I — Resistor values (KΩ) for standard output voltages

Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)			Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	13, 16, 17 18, 21, 23	4.12	3.01	1.8	0.5	1.2	+100	19	3.57	102	2.2	10	91
+ 5	13, 16, 17 18, 21, 23	2.15	4.99	0.75	0.5	2.2	+250	19	3.57	255	2.2	10	240
+ 6	13, 16, 17 18, 21, 23	1.15	6.04	0.5	0.5	2.7	- 6(°°)	15	3.57	2.43	1.2	0.5	0.75
+ 9	14, 16, 17 18, 21, 23	1.87	7.15	0.75	1	2.7	- 9	15	3.48	5.36	1.2	0.5	2
+12	14, 16, 17 18, 21, 23	4.87	7.15	2	1	3	- 12	15	3.57	8.45	1.2	0.5	3.3
+15	14, 16, 17 18, 21, 23	7.87	7.15	3.3	1	3	- 15	15	3.65	11.5	1.2	0.5	4.3
+28	14, 16, 17 18, 21, 23	21	7.15	5.6	1	2	- 28	15	3.57	24.3	1.2	0.5	10
+45	19	3.57	48.7	2.2	10	39	- 45	20	3.57	41.2	2.2	10	33
+75	19	3.57	78.7	2.2	10	68	-100	20	3.57	97.6	2.2	10	91
							-250	20	3.57	249	2.2	10	240

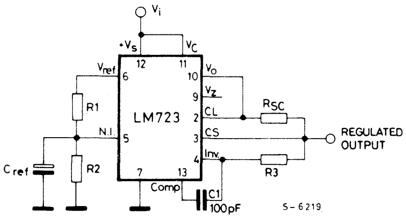
Note: (°) Replace R_1/R_2 divider with the circuit of fig. 24.
(°°) V^+ must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 13, 17, 18, 21, 23, 16 $V_O = \left[V_{ref} \times \frac{R_2}{R_1 + R_2}\right]$	Outputs from +4 to +250 volts Fig. 19 $V_O = \left[\frac{V_{ref}}{2} \times \frac{R_2 - R_1}{R_1}\right]; R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 14, 16, 17, 18, 21, 23 $V_O = \left[V_{ref} \times \frac{R_1 + R_2}{R_2}\right]$	Output from -6 to -250 volts Fig. 15, 20 $V_O = \left[\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}\right]; R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = \left[\frac{V_O\ R_3}{R_{sc}\ R_4} + \frac{V_{SENSE}\ (R_3 + R_4)}{R_{sc}\ R_4}\right]$ $I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}\right]$

APPLICATION INFORMATION (Pin numbers relative to the plastic package)

Fig. 13 - Basic low voltage regulator
(V_o = 2 to 7V)



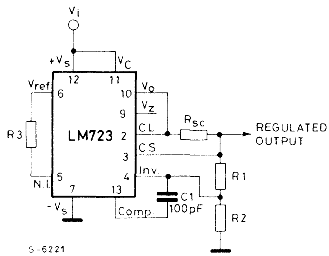
NOTE: R3 = $\frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) . . . . . . .0.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .1.5 mV

Fig. 14 - Basic high voltage regulator
(V_o = 7 to 37V)



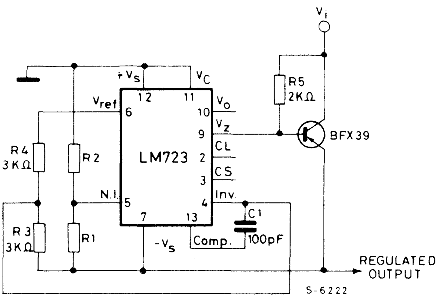
NOTE: $\frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . . .1.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .4.5 mV

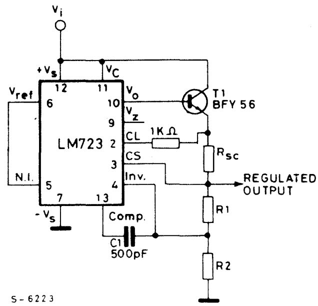
Fig. 15 - Negative voltage regulator



Typical performance

Regulated Output Voltage . . . .-15V
Line Regulation (ΔV_i = 3V) . . . . .1 mV
Load Regulation (ΔI_O = 100 mA) . . . .2 mV

Fig. 16 - Positive voltage regulator (External NPN Pass Transistor)



Typical performance

Regulated Output Voltage . . . .+15V
Line Regulation (ΔV_i = 3V) . . . . . . .1.5 mV
Load Regulation (ΔI_O = 1A) . . . . . . 15 mV

LINEAR INTEGRATED CIRCUITS

LM741
LM741A
LM741C

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIERS

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP

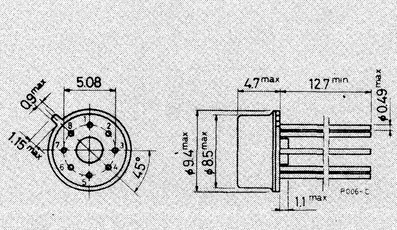
The LM741 series consists of general purpose operational amplifiers, intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the LM741 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers, and general feedback applications.

ABSOLUTE MAXIMUM RATINGS		LM741/741A	LM741C
V_s	Supply voltage	± 22V	± 18V
V_i (1)	Input voltage	± 15V	± 15V
ΔV_i	Differential input voltage	± 30V	± 30V
T_{op}	Operating temperature	-55 to 125°C	0 to 70°C
	Output short circuit duration (2)	indefinite	indefinite
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	665 mW
T_{stg}	Storage temperature	-65 to 150°C	-55 to 150°C

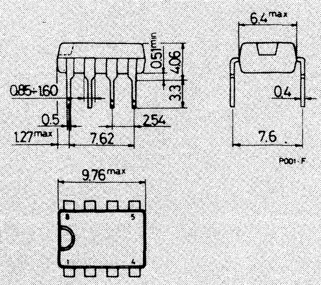
1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage.
2) The short circuit duration is limited by thermal dissipation.

MECHANICAL DATA

Dimensions in mm



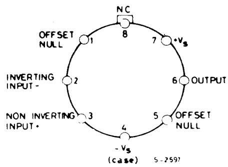
TO-99

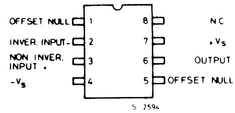


Minidip

LM741
LM741A
LM741C

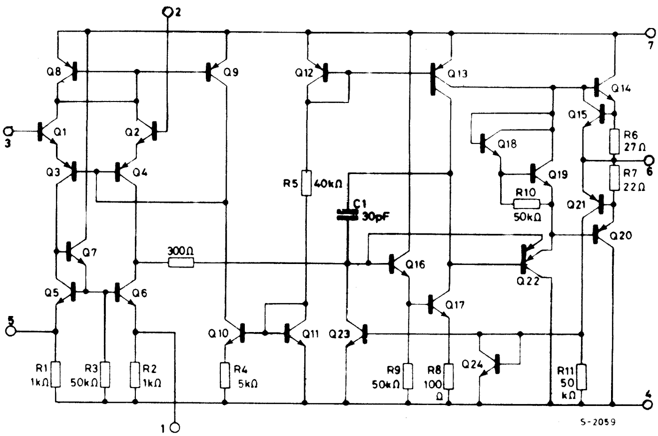
CONNECTION DIAGRAMS AND ORDERING NUMBERS





Type	TO-99	Minidip
LM 741	LM 741 H	–
LM 741A	LM 741 AH	–
LM 741C	LM 741 CH	LM 741 CN

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-99	Minidip
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	155 °C/W	120 °C/W

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LM 741			LM 741A			LM 741C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb} = 25°C										
		$R_g \leq 10\ k\Omega$		1	5					2	6	mV
		$R_g \leq 50\ \Omega$					0.8	3				mV
		$T_{amb} = T_{min}$ to T_{max}										
		$R_g \leq 10\ k\Omega$			6						7.5	mV
		$R_g \leq 50\ \Omega$						4				mV
ΔV_{os}	Input offset voltage adjust. range	$V_s = \pm 20V$				±10						mV
		$V_s = \pm 15V$ T_{amb} = 25°C		±15						±15		
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift							15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb} = 25°C		20	200		3	30		20	200	nA
		$T_{amb} = T_{min}$ to T_{max}		85	500			70			300	nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.5				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb} = 25°C		80	500		30	80		80	500	nA
		$T_{amb} = T_{min}$ to T_{max}			1.5			0.21			0.8	µA
R_i	Input resistance	T_{amb} = 25°C	0.3	2		1	6		0.3	2		MΩ
		$T_{amb} = T_{min}$ to T_{max}				0.5						MΩ
V_i	Input voltage range	$T_{amb} = T_{min}$ to T_{max}	±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb} = 25°C $R_L \geq 2\ k\Omega$ $V_s = \pm 15V$ $V_o = \pm 10V$	94	106		94			86	106		dB
		$T_{amb} = T_{min}$ to T_{max} $R_L \geq 2\ k\Omega$										
		$V_s = \pm 15V$ $V_o = \pm 10V$	88			90			84			dB
		$V_s = \pm 5V$ $V_o = \pm 2V$				80						
V_o	Output voltage swing	$V_s = \pm 15V$										
		$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		±10	±13		V
I_{sc}	Output short circuit current	T_{amb} = 25°C		25		10	25	35		25		mA
		$T_{amb} = T_{min}$ to T_{max}				10		40				mA
CMR	Common mode rejection	$V_s = \pm 20V$ $R_g \leq 10\ k\Omega$ $V_{CM} = \pm 12V$	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 50\Omega$ $V_s = \pm 5$ to $\pm 20V$				86	96					dB
		$R_g \leq 10k\Omega$ $V_s = \pm 5$ to $\pm 15V$	77	96					77	96		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LM 741			LM 741A			LM 741C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain)	T_{amb}= 25°C										
	Rise time			0.3			0.25	0.8		0.3		μs
	Overshoot			5			6	20		5		%
B	Bandwidth	T_{amb}= 25°C				0.437	1.5					MHz
SR	Slew rate	T_{amb}= 25°C		0.5		0.3	0.7			0.5		V/μs
I_s	Supply current	T_{amb}= 25°C		1.7	2.8					1.7	2.8	mA
P_{tot}	Power consumption	T_{amb}= 25°C										
		V_s= ±20V					80	150				mW
		V_s= ±15V		50	85					50	85	mW
		V_s= ±20V										
		T_{amb}= T_{min}						165				mW
		T_{amb}= T_{max}						135				mW
		V_s= ±15V										
		T_{amb}= T_{min}		60	100							mW
		T_{amb}= T_{max}		45	75							mW

Note: These specifications, unless otherwise specified, apply for V_s= ±15V and T_{amb}= -55 to 125°C for LM 741 and LM741A. For the LM 741C these specifications apply for T_{amb}= 0 to 70°C.

Fig. 1 - Open loop voltage gain vs. frequency

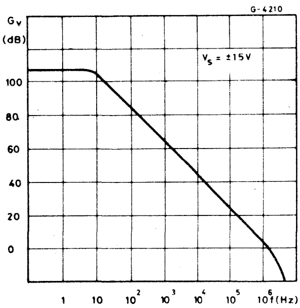


Fig. 2 - Open loop phase response vs. frequency

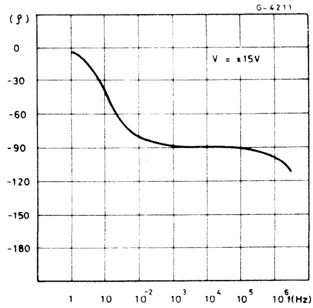
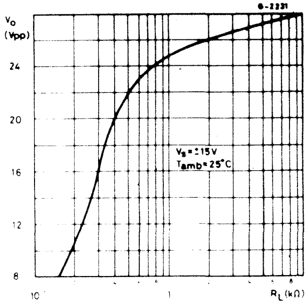


Fig. 3 - Output voltage swing vs. load resistance



LINEAR INTEGRATED CIRCUITS

LM748
LM748C

OPERATIONAL AMPLIFIERS

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP
- SLEW-RATE = 5.5V/μs (G_v = 10, C_C = 3.5 pF)

The LM748 series consists of general purpose operational amplifiers, intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "Latch-up" tendencies make the LM748 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers and general feedback applications. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor.

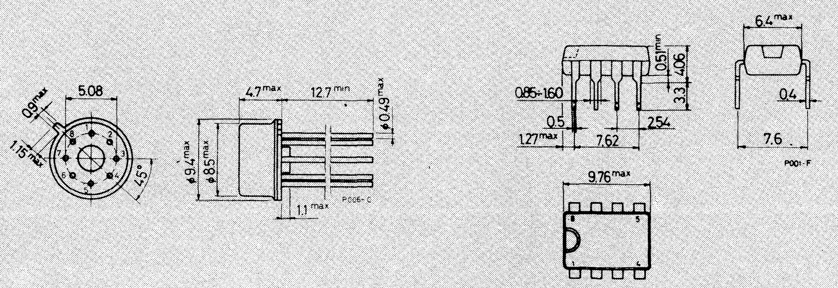
ABSOLUTE MAXIMUM RATINGS

		LM748	LM748C
V_s	Supply voltage	± 22V	± 22V
V_i (1)	Input voltage	± 15V	± 15V
ΔV_i	Differential input voltage	± 30V	± 30V
T_{op}	Operating temperature	-55 to 125 °C	0 to 70 °C
	Output short circuit duration (2)	indefinite	indefinite
P_{tot}	Power dissipation at T_{amb} = 70°C: **TO-99**	520 mW	520 mW
	Minidip	–	665 mW
T_{stg}	Storage temperature	65 to 150 °C	-55 to 150 °C

1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation.

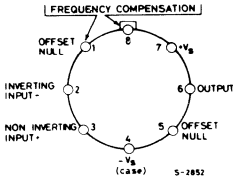
MECHANICAL DATA

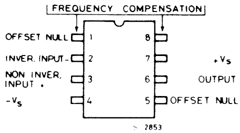
Dimensions in mm



TO-99 **Minidip**

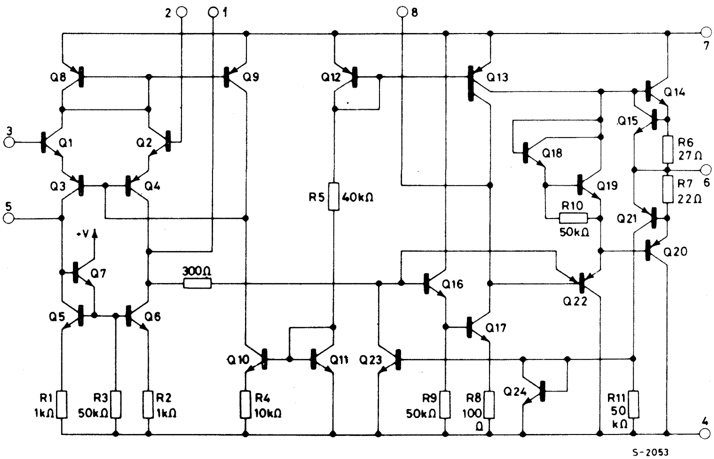
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-99	Minidip
LM 748	LM 748H	—
LM 748C	LM 748 CH	LM 748 CN

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	Minidip
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions		LM748			LM748C			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C $R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$			1	5		2	6	mV
		T_{amb}= T_{min} to T_{max} $R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$			1	6			7.5	mV
ΔV_{os}	Input offset voltage adjust. range	T_{amb}= 25°C			±15			±15		mV
I_{os}	Input offset current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}			20 50	200 500		20	200 300	nA nA
I_b	Input bias current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}			80	500 1.5		80	500 0.8	nA µA
R_i	Input resistance	T_{amb}= 25°C		0.3	2		0.3	2		MΩ
V_i	Input voltage range			±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V		94	104		86	104		dB
		T_{amb}= T_{min} to T_{max} $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V		88			84			dB
V_o	Output voltage swing	V_s= ±15V $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
I_{sc}	Output short circuit current				25			25		mA
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$ V_{CM}= ±12V		70	90		70	90		dB
SVR	Supply voltage rejection	V_s= ±5 to ± 20V $R_g \leq 10\ k\Omega$		76	90		76	90		dB
SR	Slew rate	T_{amb}= 25°C $R_L \geq 2\ k\Omega$	G_v= 1		0.5			0.5		V/µs
			G_v= 10*		5.5			5.5		V/µs

* C_C = 3.5 pF

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	LM748			LM748C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain) Rise time Overshoot	T_{amb}= 25°C V_i= 20 mV C_C= 30 pF R_L= 2 kΩ $C_L \leq$ 100 pF		0.2 5			0.2 5		μs %
I_s	Supply current	T_{amb}= 25°C		1.9	2.8		1.9	2.8	mA
P_S	Power consumption	T_{amb}= 25°C V_s= ±15V		60	85		60	85	mW
		V_s= ±15V T_{amb}= T_{min} T_{amb}= T_{max}		60 45	100 75		60	100	mW mW

Note: These specifications, unless otherwise specified, apply for V_s= ±15V and T_{amb}= -55 to 125°C for LM748. For LM748C these specifications apply for T_{amb}= 0 to 70°C (C_c = 30 pF).

Fig. 1 - Voltage offset null circuits

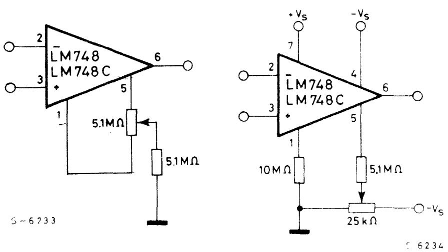


Fig. 2 - Transient response test circuit

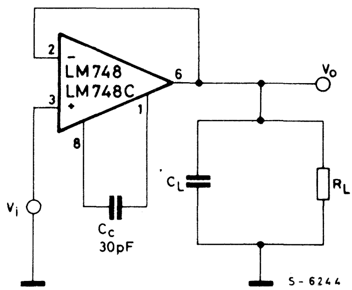


Fig. 3 - Input noise voltage vs. frequency

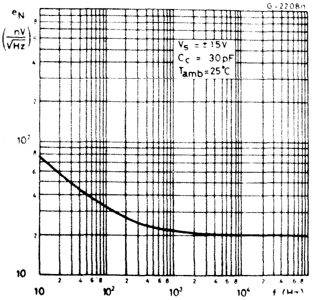


Fig. 4 - Input noise current vs. frequency

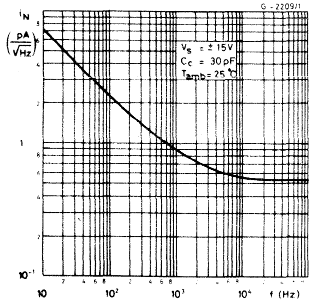


Fig. 5 - Broadband noise for various bandwidths

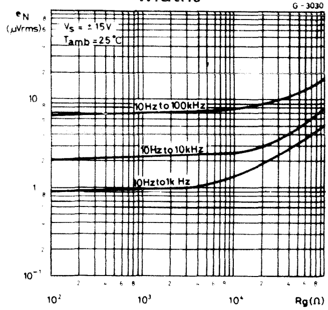


Fig. 6 - Open loop frequency and phase response vs. frequency

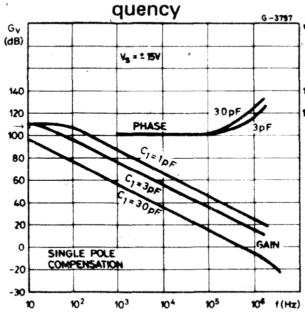


Fig. 7 - Output voltage swing vs. frequency

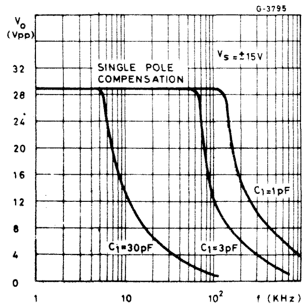


Fig. 8 - Slew-rate

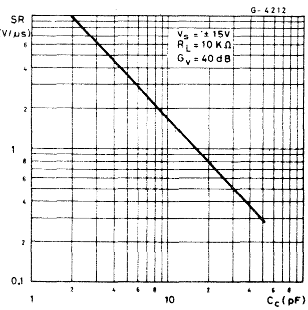


Fig. 9 - Compensation capacitance vs. closed loop voltage gain

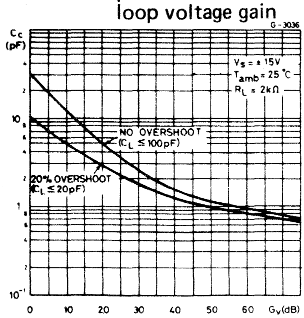


Fig. 10 - Input resistance and input capacitance vs. frequency

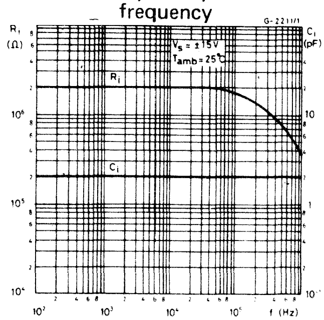
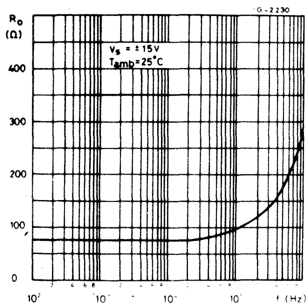


Fig. 11 - Output resistance vs. frequency



LM2930A

LINEAR INTEGRATED CIRCUITS

ADVANCE DATA

VERY LOW DROP VOLTAGE REGULATOR

- INPUT/OUTPUT DROP TYP. 0.2V at 150 mA
- OUTPUT CURRENT IN EXCESS OF 400 mA
- 40V LOAD DUMP PROTECTION
- -40V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

The LM2930A is an improved version of the LM2930 5V voltage regulator which features an output current rating of 400mA with a dropout voltage of typically 0.4V. At 150mA the dropout voltage falls to 0.2V. Moreover, the LM2930A includes load dump protection plus reverse polarity protection, input overvoltage protection, thermal shutdown and foldback current limiting. Designed primarily for automotive applications, the LM2930A protects both itself and the load from load dump transients and incorrect battery connection. The low voltage drop of this device allows correct operation even during starting when the battery voltage can fall below 6V. The LM2930A is available in a TO-220 plastic power package.

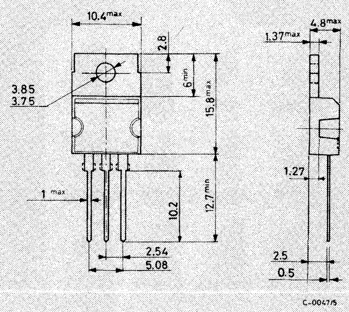
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	26	V
	Overvoltage protection (t = 100ms)	± 40	V
T_{op}	Operating temperature range	-40 to +85	°C
T_j	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

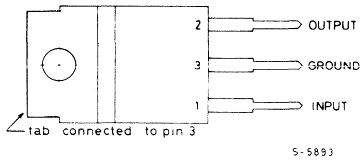
ORDERING NUMBER: LM2930A

MECHANICAL DATA

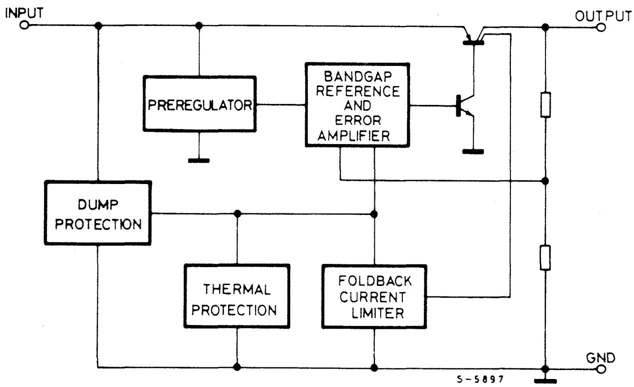
Dimensions in mm



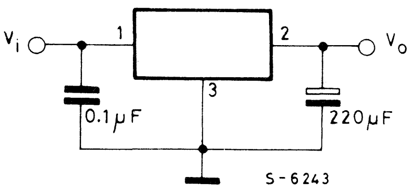
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, I_o = 150mA, T_j = 25°C unless otherwise specified).

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	$6V \leq V_i \leq 26V$, $5mA \leq I_o \leq 150mA$ $-40°C \leq T_j \leq +125°C$	4.5	5	5.5	V
ΔV_o	Line regulation	$9V \leq V_i \leq 16V$, I_o = 5mA		7	25	mV
		$6V \leq V_i \leq 26V$, I_o = 5mA		30	80	mV
ΔV_o	Load regulation	$5mA \leq I_o \leq 150mA$		14	50	mV
R_o	Output impedance	$100mA_{DC}$ & 10mArms, 100Hz - 10KHz		200		mΩ
I_d	Quiescent current	I_o = 10mA I_o = 150mA		4 18	7 40	mA mA
e_N	Output noise voltage	10Hz - 100KHz		140		μVrms
	Long term stability			20		mV/ 1000 hr
SVR	Supply voltage rejection	f_o = 120Hz		56		dB
I_o	Current limit			650		mA
V_i-V_o	Dropout voltage	I_o = 150mA I_o = 400mA		0.2 0.4	0.5	V V

LINEAR INTEGRATED CIRCUITS

LM2931A

ADVANCE DATA

VERY LOW DROP VOLTAGE REGULATOR

- VERY LOW QUIESCENT CURRENT
- OUTPUT CURRENT IN EXCESS OF 400mA
- INPUT/OUTPUT DROP TYP. 0.2V at 150 mA
- REVERSE POLARITY PROTECTION
- 60V LOAD DUMP PROTECTION
- -60V TRANSIENT PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

The LM2931A is an improved version of the LM2931 5V voltage regulator which features an output current rating of 400mA with a dropout voltage of typically 0.4V. At 150mA the dropout voltage falls to 0.2V. A special feature of this device is the low quiescent current of 2mA at 10mA output current which makes it ideal for standby and backup applications. Designed for automotive applications, the LM2931A protects itself and the load from ±60V load dump transients, battery reversal and input overvoltage. It also includes a thermal shutdown circuit and a foldback current limiter. The low voltage drop of the LM2931A allows correct operation of 5V automotive equipment during starting when the battery voltage can fall below 6V. The LM2931A is available in a TO-220 plastic power package.

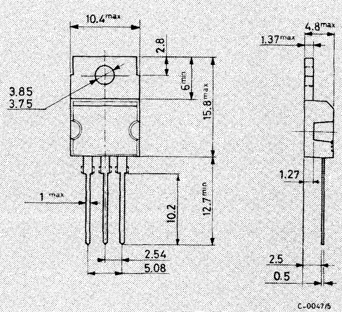
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	26	V
	Overvoltage protection (t = 100ms)	± 60	V
T_{op}	Operating temperature range	-40 to +85	°C
T_j	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

ORDERING NUMBER: LM2931A

MECHANICAL DATA

Dimensions in mm



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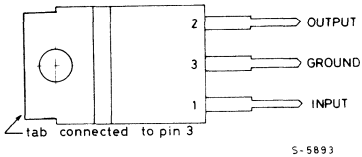
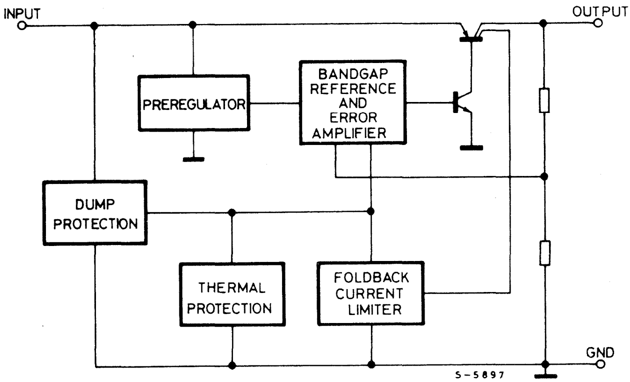
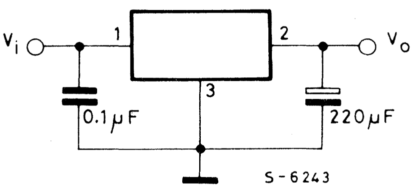
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	4	°C/W

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, I_o = 10mA, T_j = 25°C unless otherwise specified).

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	$6V \leq V_i \leq 26V$, $I_o \leq 150$ mA $-40°C \leq T_j \leq +125°C$	4.75	5	5.25	V
ΔV_o	Line regulation	$9V \leq V_i \leq 16V$		2	10	mV
		$6V \leq V_i \leq 26V$		4	30	mV
ΔV_o	Load regulation	$5mA \leq I_o \leq 150mA$		14	50	mV
R_o	Output impedance	$100mA_{DC}$ & 10mArms, 100Hz - 10KHz		200		mΩ
I_d	Quiescent current	I_o = 10mA $6V \leq V_i \leq 26V$ $-40°C \leq T_j \leq +125°C$ I_o = 150mA, V_i = 14V, T_j = 25°C		0.8 20	2 40	mA mA
e_N	Output noise voltage	10Hz - 100KHz		500		μVrms
	Long term stability			20		mV/ 1000 hr
SVR	Supply voltage rejection	f_o = 120Hz		80		dB
V_i-V_o	Dropout voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	0.1 0.4	V V V
I_o	Current limit			650		mA

LS 101
LS 201
LS 301

LINEAR INTEGRATED CIRCUITS

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

- GUARANTED DRIFT CHARACTERISTICS
- SLEW RATE OF 10V/µs AS A SUMMING AMPLIFIER
- UNITY GAIN PHASE COMPENSATION WITH A SINGLE 30 pF CAPACITOR
- 3 mV MAX OFFSET VOLTAGE OVER TEMPERATURE RANGE
- 100 nA MAX INPUT BIAS CURRENT OVER TEMPERATURE RANGE

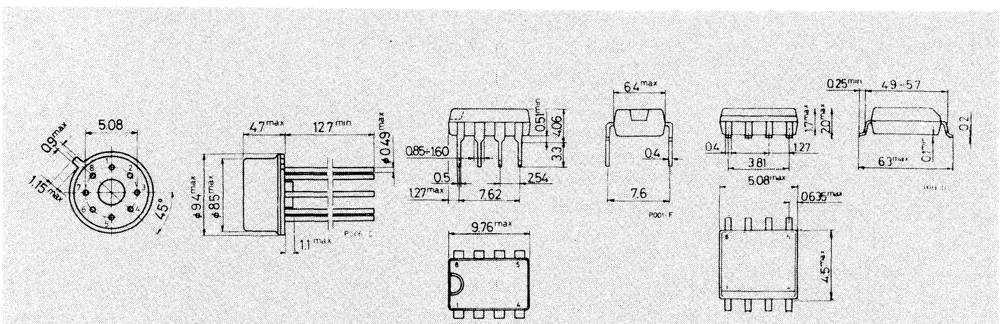
The LS 101 series consists of high performance operational amplifiers, intended for a wide range of analog applications, where tailoring of frequency characteristics is desirable. The LS 101 series is short circuit protected and has the same pin configuration as the LS 141 and LS 148. Absence of latch-up and high common mode voltage range make the LS 101 series ideal for use as voltage followers. In addition, the LS 101 series provides better accuracy and lower noise in high impedance circuitry: the low input current also makes it particularly well suited for long interval integrators, timers, sample and hold circuits and low frequency generators. The LS 101 series is also available with hermetic gold chip (8000 series), particularly suitable for professional and telecom applications, wherever very high MTBF are required.

ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	µpackage
V_s	Supply voltage for **LS 101/101A/201/201A**		± 22 V	
	for **LS 301A**		± 18 V	
V_i (1)	Input voltage		± 15 V	
ΔV_i	Differential input voltage		± 30 V	
T_{op}	Operating temperature for **LS 101/LS 101A**		-55 to 125 °C	
	for **LS 201A**		-25 to 85 °C	
	for **LS 201/LS 301A**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb} = 70 °C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C

(1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage.
(2) The short circuit duration is limited by thermal dissipation.

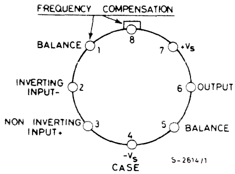
MECHANICAL DATA

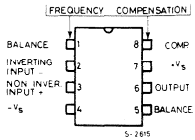
Dimensions in mm

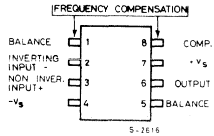


TO-99 Minidip SO-8

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

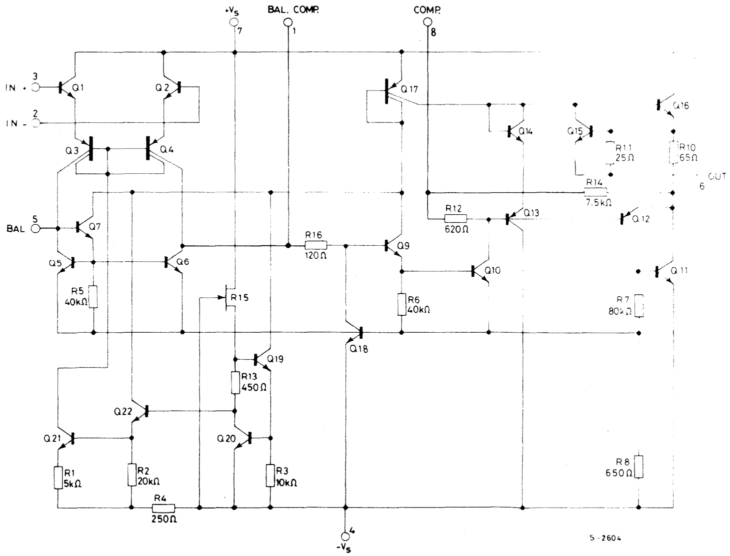






Type	TO-99	Minidip	SO-8
LS 101	LS 101 TB	–	–
LS 101A	LS 101 ATB	–	–
LS 201	LS 201 TB	LS 201B	LS 201M
LS 201A	LS 201 ATB	–	–
LS 301A	LS 301 ATB	LS 301AB	LS 301AM
LS 8101	–	–	LS 8101M
LS 8101A	–	–	LS 8101AM
LS 8201	–	–	LS 8201M
LS 8201A	–	–	LS 8201AM
LS 8301A	–	–	LS 8301AM

SCHEMATIC DIAGRAM



THERMAL DATA

THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25x16x0.6 mm)

ELECTRICAL CHARACTERISTICS* for LS 101 and LS 201

Parameter		Test conditions	LS 101			LS 201			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 10\ k\Omega$ $T_{amb} = 25°C$		 1	6 5		 2	10 7.5	mV mV
$\frac{\Delta V_{os}}{\Delta T}$	Average temperat. coefficient of input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$		6 3			10 6		μV/°C μV/°C
I_{os}	Input offset current	$T_{amb} = 25°C$ $T_{amb} = T_{max}$ $T_{amb} = T_{min}$		40 10 100	200 200 500		100 50 150	500 400 750	nA nA nA
I_b	Input bias current	 $T_{amb} = 25°C$		 0.12	1.5 0.5		 0.25	2 1.5	μA μA
R_i	Input resistance	$T_{amb} = 25°C$	0.3	0.8		0.1	0.4		MΩ
V_i	Input voltage range	$V_s = \pm15V$	± 12			± 12			V
G_v	Large signal voltage gain	$V_s = \pm15V$ $V_o = \pm10V$ $R_L \geq 2\ k\Omega$	88			83			dB
		$V_s = \pm15V$ $V_o = \pm10V$ $R_L \geq 2\ k\Omega$ $T_{amb} = 25°C$	94	104		86	103		dB
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	90		65	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	70	90		70	90		dB
V_o	Output voltage swing	$V_s = \pm\ 15V$ $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	 ± 12 ± 10	 ± 14 ± 13		 ± 12 ± 10	 ± 14 ± 13		 V V
I_s	Supply current	$V_s \pm 20V$		1.8	3		1.8	3	mA

* These specifications, unless otherwise specified, apply for $C_1 = 30$ pF, $V_s = \pm5$ to $\pm20V$ and $T_{amb} = -55$ to 125 °C (LS 101/LS 101A), $T_{amb} = -25$ to 85 °C (LS 201A) and $T_{amb} = 0$ to 70 °C (LS 201); $V_s = \pm5$ to $\pm15V$ and $T_{amb} = 0$ to 70 °C (LS 301A).

ELECTRICAL CHARACTERISTICS* for LS 101A, LS 201A and LS 301A

Parameter		Test conditions	LS 101A/LS 201A			LS 301A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leqslant 10\ k\Omega$ $R_g \leqslant 10\ k\Omega$ $T_{amb} = 25°C$		 0.7	3 2		 2	10 7.5	mV mV
$\frac{\Delta V_{os}}{\Delta T}$	Average temperat. coefficient of input offset voltage	$R_g \leqslant 10\ k\Omega$		3	15		6	30	$\mu V/°C$
I_{os}	Input offset current	$T_{amb} = 25°C$		 1.5	20 10		 3	70 50	nA nA
$\frac{\Delta I_{os}}{\Delta T}$	Average temperat. coefficient of input offset current	$T_{amb} = 25°C$ to T_{max} $T_{amb} = T_{min}$ to $25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
I_b	Input bias current	 $T_{amb} = 25°C$		 30	0.1 75		 70	0.3 250	μA nA
R_i	Input resistance	$T_{amb} = 25°C$	1.5	4		0.5	2		MΩ
V_i	Input voltage range	$V_s = \pm 20V$ $V_s = \pm 15V$	± 15			 ±12			V V
G_v	Large signal voltage gain	$V_s = \pm 15V$ $V_o = \pm 10V$ $R_L \geqslant 2\ k\Omega$	88			83			dB
		$V_s = \pm 15V$ $V_o = \pm 10V$ $R_L \geqslant 2\ k\Omega$ $T_{amb} = 25°C$	94	104		86	104		dB
CMR	Common mode rejection	$R_g \leqslant 10\ k\Omega$	80	96		70	90		dB
SVR	Supply voltage rejection	$R_g \leqslant 10\ k\Omega$	80	96		70	96		dB
V_o	Output voltage swing	$V_s = \pm 15V$ $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	 ± 12 ± 10	 ± 14 ± 13		 ± 12 ± 10	 ± 14 ± 13		 V V
I_s	Supply current	$V_s = \pm 20V$ $T_{amb} = T_{max}$		1.2	2.5				mA
		$T_{amb} = 25°C$ $V_s = \pm 20V$ $V_s = \pm 15V$		 1.8	 3		 1.8	 3	 mA mA

* These specifications, unless otherwise specified, apply for $C_1 = 30$ pF, $V_s = \pm 5$ to $\pm 20V$ and $T_{amb} = -55$ to 125 °C (LS 101/LS 101A), $T_{amb} = -25$ to 85 °C (LS 201A) and $T_{amb} = 0$ to 70 °C (LS 201); $V_s = \pm 5$ to $\pm 15V$ and $T_{amb} = 0$ to 70 °C (LS 301A).

Guaranteed characteristics (LS 101/LS 201)

Fig. 1 - Input voltage range vs. supply voltage

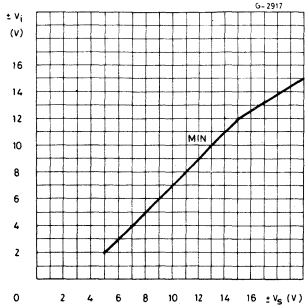


Fig. 2 - Output voltage swing vs. supply voltage

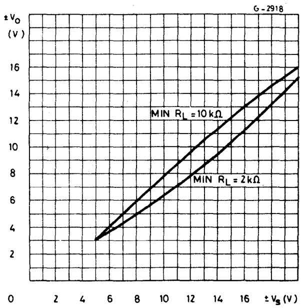
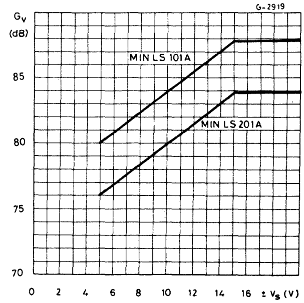


Fig. 3 -- Voltage gain vs. supply voltage



Guaranteed characteristics (LS 101A/LS 201A)

Fig. 4 - Input voltage range vs. supply voltage

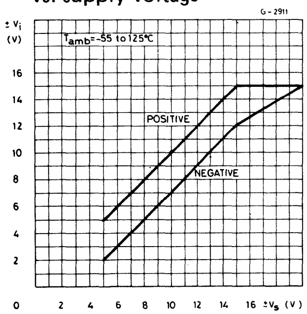


Fig. 5 - Output voltage swing vs. supply voltage

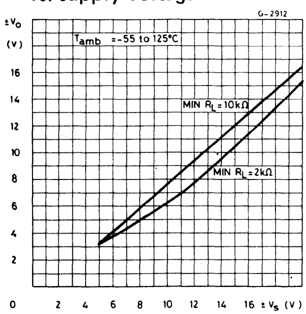
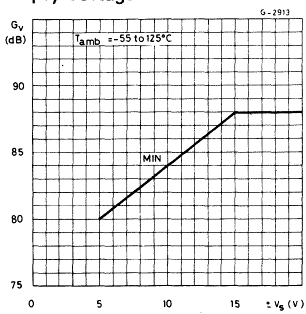


Fig. 6 - Voltage gain vs. supply voltage



Guaranteed characteristics (LS 301A)

Fig. 7 - Input voltage range vs. supply voltage

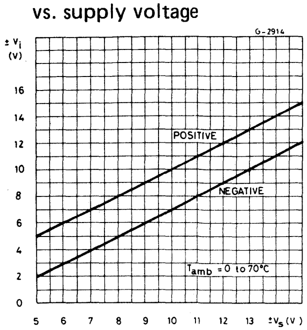


Fig. 8 - Output voltage swing vs. supply voltage

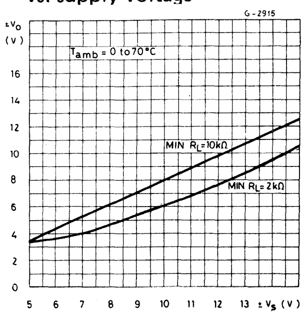


Fig. 9 - Voltage gain vs. supply voltage

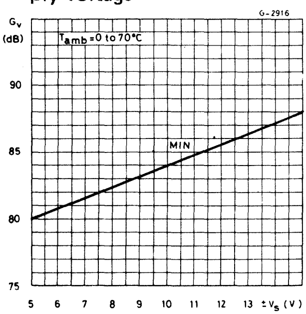


Fig. 10 - Input bias current vs. ambient temperature (for LS 101A/201A/301A)

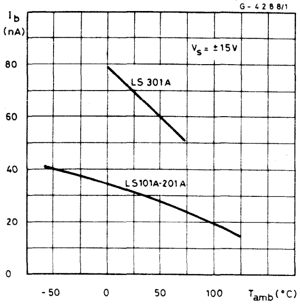


Fig. 11 - Input offset current vs. ambient temperature (for LS 101A/201A/301A)

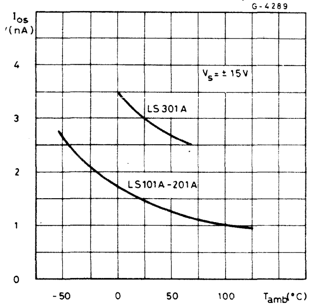


Fig. 12 - Input bias current vs. ambient temperature (for LS 101/201)

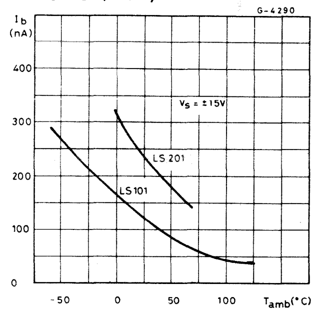


Fig. 13 - Input offset current vs. ambient temperature (for LS 101/201)

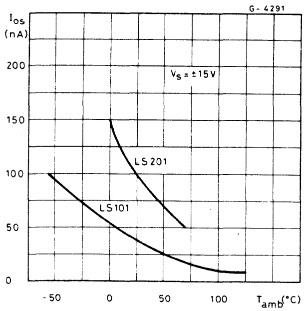


Fig. 14 - Supply current vs. supply voltage

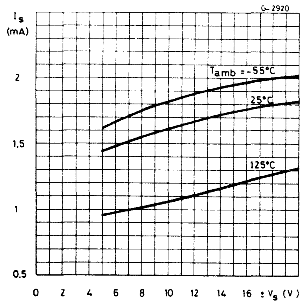


Fig. 15 - Voltage gain vs. supply voltage

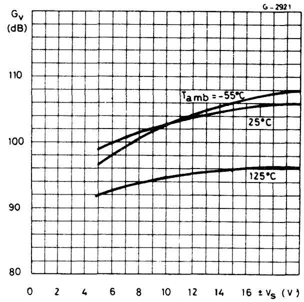


Fig. 16 - Output voltage swing vs. output current

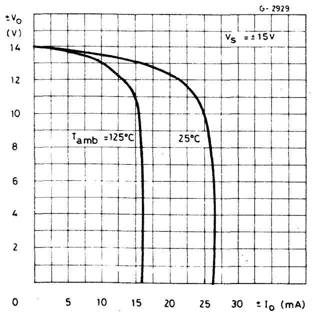


Fig. 17 - Input noise voltage vs. frequency

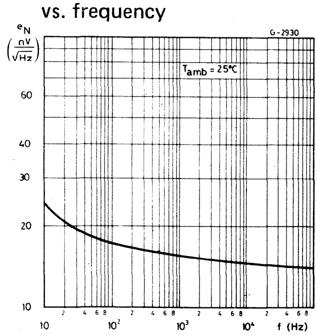
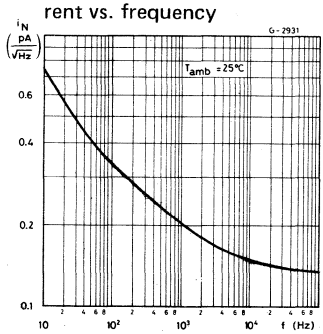


Fig. 18 - Input noise current vs. frequency



OPERATIONAL AMPLIFIER COMPENSATION

SINGLE POLE

Fig. 19

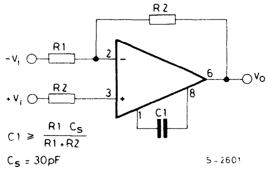


Fig. 20 - Open loop frequency response

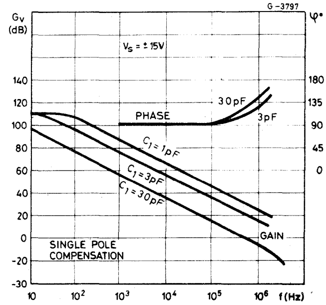
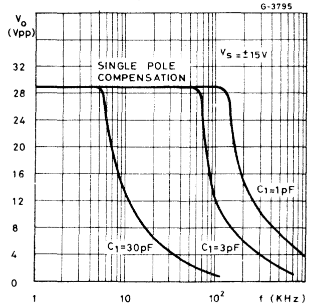


Fig. 21 - Large signal frequency response



TWO POLE

Fig. 22

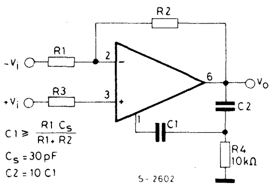


Fig. 23 - Open loop frequency response

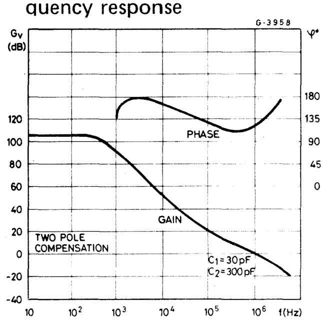
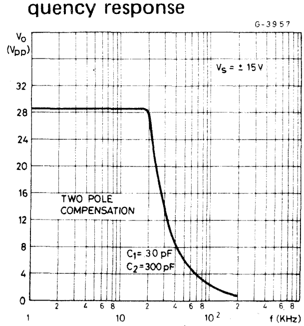


Fig. 24 - Large signal frequency response



FEED FORWARD

Fig. 25

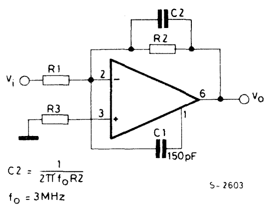


Fig. 26 - Open loop frequency response

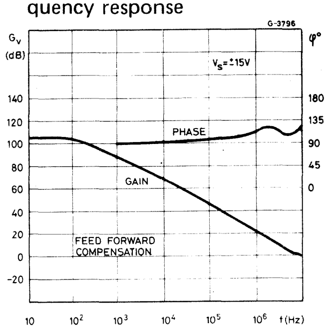


Fig. 27 - Large signal frequency response

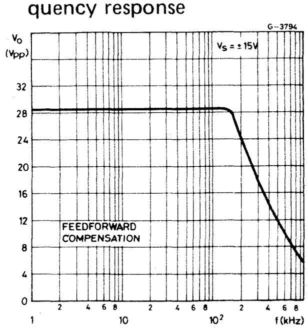


Fig. 28 - Single pole compensation pulse response

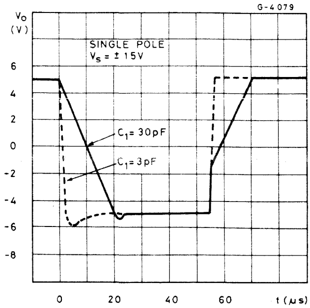


Fig. 29 - Two pole compensation pulse response

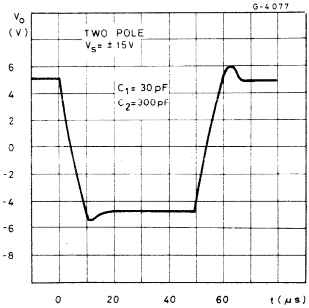
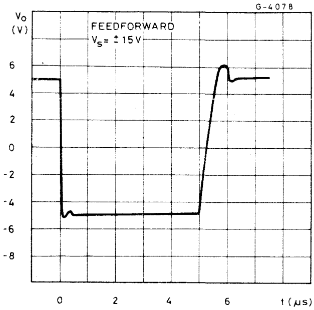


Fig. 30 - Feed forward pulse response



TYPICAL APPLICATIONS

Fig. 31 - Inverting amplifier with balancing circuit

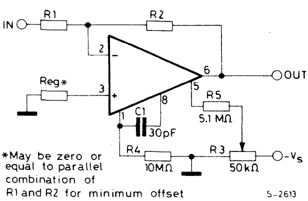


Fig. 32 - Integrator with bias current compensation

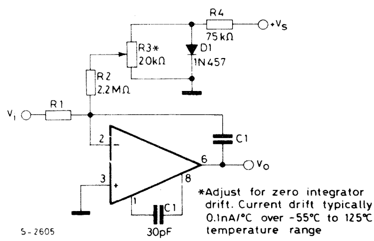


Fig. 33 - Standard compensation and offset balancing circuit

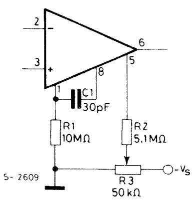
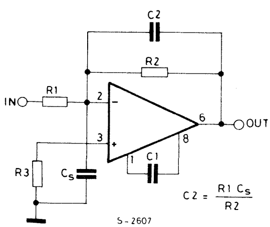


Fig. 34 - Compensation for stray input capacitances or large feedback resistor



TYPICAL APPLICATIONS (continued)

Fig. 35 - Protecting against gross fault conditions

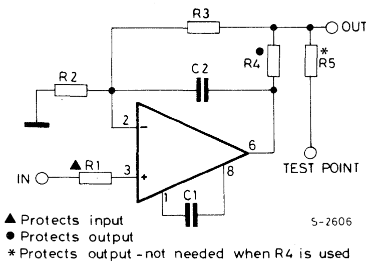


Fig. 36 - Bilateral current source

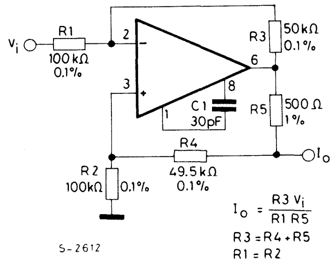
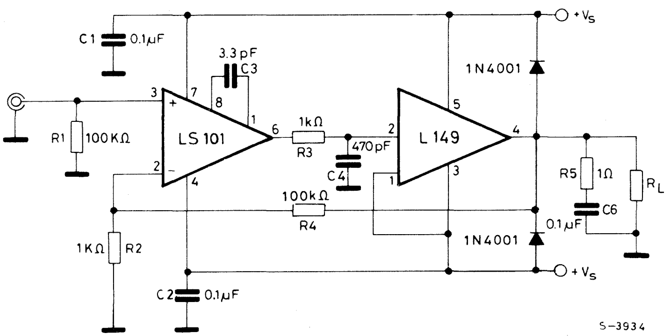


Fig. 37 - Power operational amplifier ($G_v = 40$ dB)



LINEAR INTEGRATED CIRCUITS

LS 107
LS 207
LS 307

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIERS

- LOW OFFSET CURRENT AND VOLTAGE
- LOW INPUT CURRENT
- GUARANTEED DRIFT CHARACTERISTICS

The LS 107 series consists of general purpose operational amplifiers, with the frequency compensation built into the chip. They replace pin-to-pin the LS 709, LS 101, LS 141 and LS 148.
The LS 107 series offers features similar to the LS 101A, providing better accuracy and lower noise in high impedance circuits. The low input currents allow the device to be used in slow charge applications, such as long interval integrators, slow ramps, sample and hold circuits.
The LS 107 series is available with hermetic gold chip (8000 series), particularly suitable for professional and telecom applications, wherever very high MTBF are required.

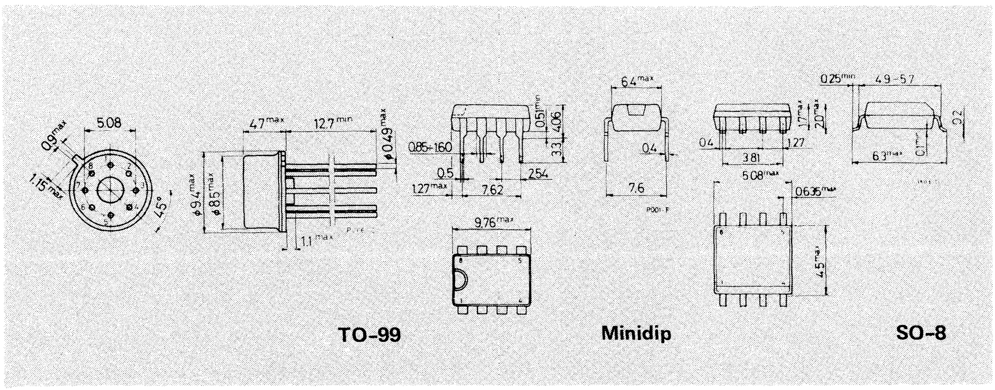
ABSOLUTE MAXIMUM RATINGS

		TO-99	Minidip	μpackage
V_s	Supply voltage for **LS 107** and **LS 207**		± 22V	
	for **LS 307**		± 18V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
T_{op}	Operating temperature for **LS 107**		-55 to 125 °C	
	for **LS 207**		-25 to 85 °C	
	for **LS 307**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70°C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C
	Lead soldering temperature	300 °C (10s)	260 °C (12s)	260 °C (5s) 235 °C (11s)

1) For supply voltages less than ±15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

MECHANICAL DATA

Dimensions in mm

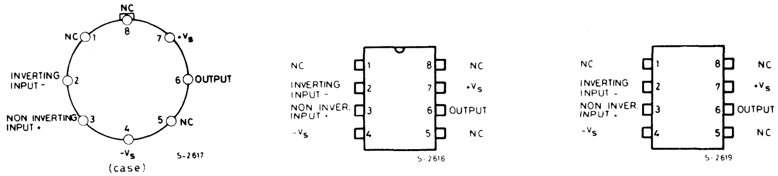


8/83

LS107
LS207
LS307

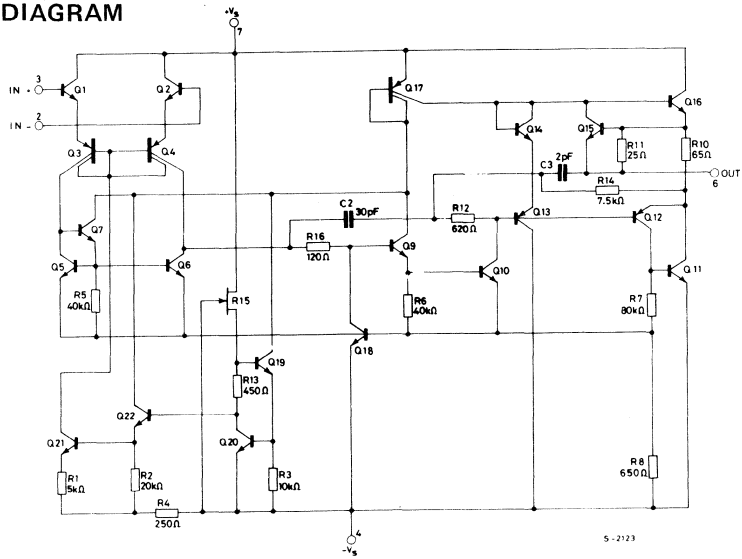
CONNECTION DIAGRAMS AND ORDERING NUMBERS

(top views)



Type	TO-99	Minidip	SO-8
LS 107	LS 107 TB	–	–
LS 207	LS 207 TB	–	–
LS 307	LS 307 TB	LS 307B	LS 307M
LS 8107	–	–	LS 8107M
LS 8207	–	–	LS 8207M
LS 8307	–	–	LS 8307M

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25x16x0.6 mm)

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 107/LS 207			LS 307			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leqslant 10\ k\Omega$			3			10	mV
		$R_g \leqslant 10\ k\Omega$ $T_{amb} = 25°C$		0.7	2		2	7.5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Average temperature coefficient of input offset voltage			3	15		6	30	μV/°C
I_{os}	Input offset current				20			70	nA
		$T_{amb} = 25°C$		1.5	10		3	50	nA
$\frac{\Delta I_{os}}{\Delta T}$	Average temperature coefficient of input offset current	$T_{amb} = 25°C$ to T_{max}		0.01	0.1		0.01	0.3	nA/°C
		$T_{amb} = T_{min}$ to $25°C$		0.02	0.2		0.02	0.6	nA/°C
I_b	Input bias current				100			300	nA
		$T_{amb} = 25°C$		30	75		70	250	nA
R_i	Input resistance	$T_{amb} = 25°C$	1.5	4		0.5	2		MΩ
G_v	Large signal voltage gain	$V_s = \pm 15V$ $V_o = \pm 10V$ $R_L \geqslant 2\ k\Omega$	88			84			dB
		$V_s = \pm 15V$ $V_o = \pm 10V$ $R_L \geqslant 2\ k\Omega$ $T_{amb} = 25°C$	94	104		88	104		dB
V_i	Input voltage range	$V_s = \pm 20V$	±15						V
		$V_s = \pm 15V$				±12			V
V_o	Output voltage swing	$V_s = \pm 15V$ $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
		$V_s = \pm 15V$ $R_L = 2\ k\Omega$	±10	±13		±10	±13		V
CMR	Common mode rejection	$R_g \leqslant 10\ k\Omega$	80	96		70	90		dB
SVR	Supply voltage rejection	$R_g \leqslant 10\ k\Omega$	80	96		70	96		dB
I_s	Supply current	$V_s = \pm 20V$							
		$T_{amb} = 25°C$		1.8	3				mA
		$T_{amb} = 125°C$		1.2	2.5				mA
		$V_s = \pm 15V$ $T_{amb} = 25°C$					1.8	3	mA

Note: These specifications, unless otherwise specified, apply for $V_s = \pm 5V$ to $\pm 20V$ and $T_{amb} = -55$ to $125°C$ for LS 107; $V_s = \pm 5V$ to $\pm 20V$ and $T_{amb} = -25$ to $85°C$ for LS 207; $V_s = \pm 5V$ to $\pm 15V$ and $T_{amb} = 0$ to $70°C$ for LS 307.

Fig. 1 - Supply current vs. supply voltage

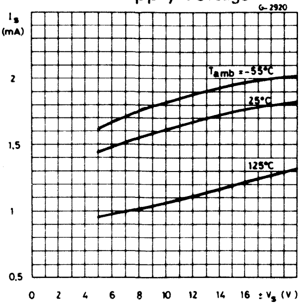


Fig. 2 - Voltage gain vs. supply voltage

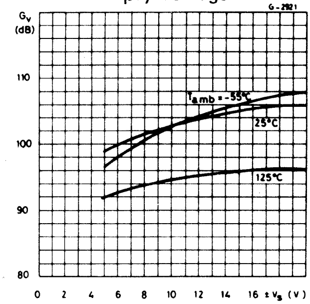


Fig. 3 - Input current vs. ambient temp.

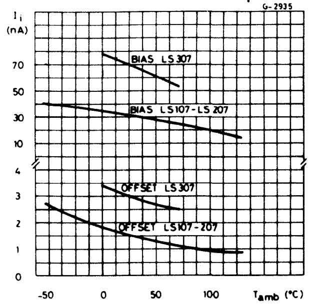


Fig. 4 - Current limiting vs. output current

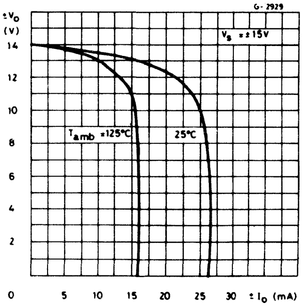


Fig. 5 - Input noise voltage vs. frequency

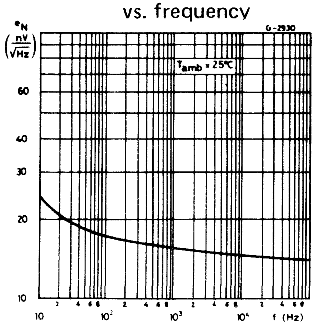


Fig. 6 - Input noise current vs. frequency

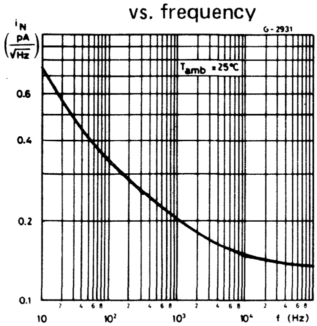


Fig. 7 - Open loop frequency response

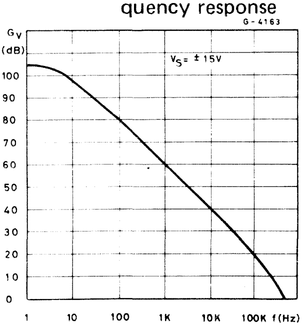


Fig. 8 - Large signal frequency response

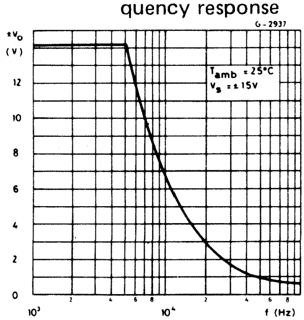
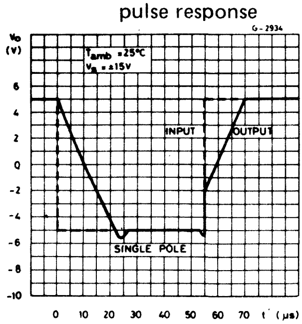


Fig. 9 - Voltage follower pulse response



Guaranteed performance characteristics (LS 107/LS 207)

Fig. 10 - Input voltage range vs. supply voltage

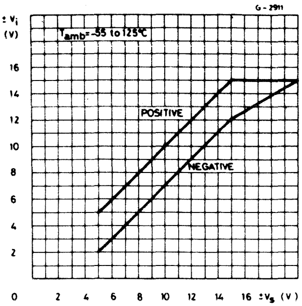


Fig. 11 - Output voltage swing vs. supply voltage

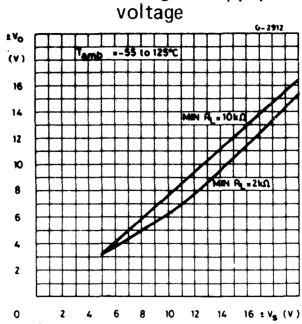
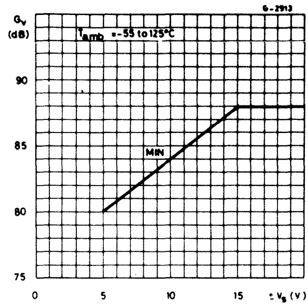


Fig. 12 - Voltage gain vs. supply voltage



Guaranteed performance characteristics (LS 307)

Fig. 13 - Input voltage range vs. supply voltage

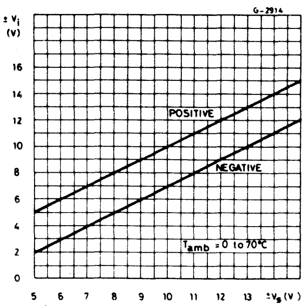


Fig. 14 - Output voltage swing vs. supply voltage

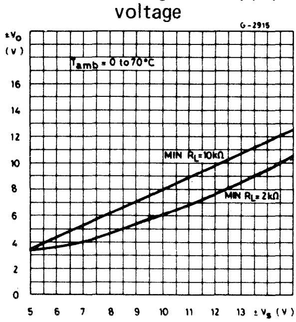
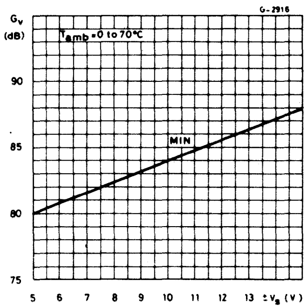
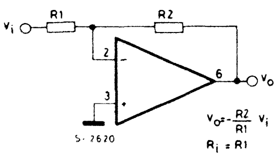


Fig. 15 - Voltage gain vs. supply voltage



TYPICAL APPLICATIONS

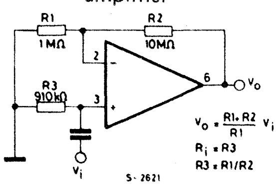
Fig. 16 - Inverting amplifier



$V_o = -\frac{R2}{R1} V_i$

$R_i = R1$

Fig. 17 - Non-inverting AC amplifier

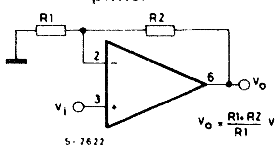


$V_o = \frac{R1+R2}{R1} V_i$

$R_i = R3$

$R3 = R1/R2$

Fig. 18 - Non-inverting amplifier



$V_o = \frac{R1+R2}{R1} V_i$

SGS

LS141
LS141A
LS141C

LINEAR INTEGRATED CIRCUITS

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIERS

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP

The LS 141 series consists of general purpose operational amplifiers, intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the LS 141 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers, and general feedback applications. The LS 141 series is available with hermetic gold chip (8000 series). This is particularly suitable for professional and telecom applications, wherever very high MTBF are required.

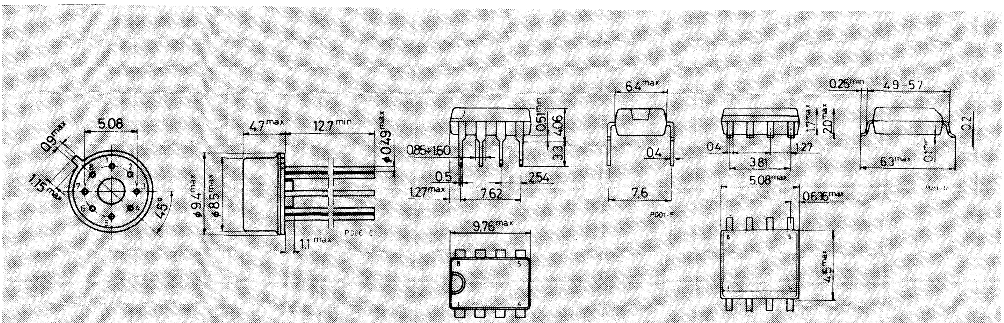
ABSOLUTE MAXIMUM RATINGS

		TO-99	Minidip	μpackage
V_s	Supply voltage for **LS 141/LS 141A**		± 22V	
	for **LS 141C**		± 18V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
T_{op}	Operating temperature for **LS 141/LS 141A**		-55 to 125°C	
	for **LS 141C**		0 to 70°C	
	Output short circuit duration(2)		indefinite	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150°C	-55 to 150°C	-55 to 150°C
	Lead soldering temperature	300°C (10s)	260°C (12s)	260°C (5s) 235°C (11s)

1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

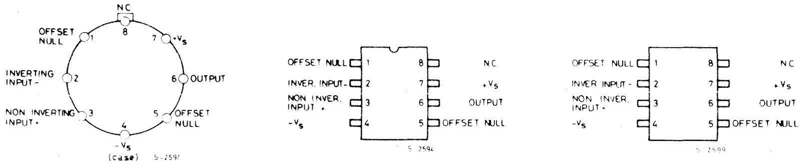
MECHANICAL DATA

Dimensions in mm



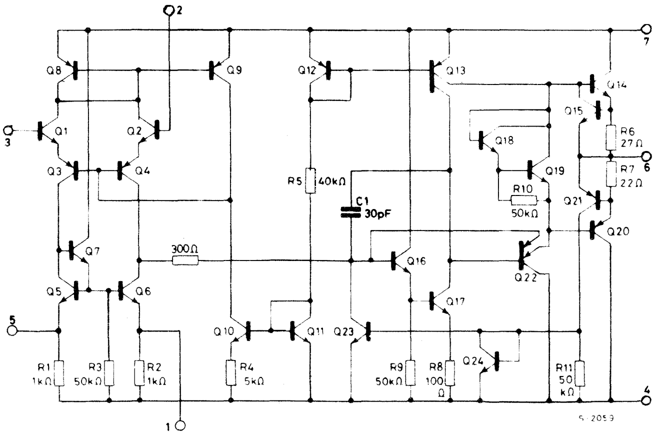
TO-99 **Minidip** **SO-8**

CONNECTION DIAGRAMS AND ORDERING NUMBERS



Type	TO-99	Minidip	SO-8
LS 141	LS 141 TB	—	—
LS 141A	LS 141 ATB	—	—
LS 141C	LS 141 CTB	LS 141 CB	LS 141 CM
LS 8141	—	—	LS 8141M
LS 8141A	—	—	LS 8141 AM
LS 8141C	—	—	LS 8141 CM

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm)

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 141			LS 141A			LS 141C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C										
		$R_g \leqslant 10\ k\Omega$		1	5					2	6	mV
		$R_g \leqslant 50\ \Omega$					0.8	3				mV
		T_{amb}= T_{min} to T_{max}										
		$R_g \leqslant 10\ k\Omega$			6						7.5	mV
		$R_g \leqslant 50\ \Omega$						4				mV
ΔV_{os}	Input offset voltage adjust. range	V_s= ± 20V				±10						mV
		V_s= ± 15V T_{amb}= 25°C		±15						±15		mV
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift							15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb}= 25°C		20	200		3	30		20	200	nA
		T_{amb}= T_{min} to T_{max}		85	500			70			300	nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.5				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb}= 25°C		80	500		30	80		80	500	nA
		T_{amb}= T_{min} to T_{max}			1.5			0.21			0.8	μA
R_i	Input resistance	T_{amb}= 25°C	0.3	2		1	6		0.3	2		MΩ
		T_{amb}= T_{min} to T_{max}				0.5						MΩ
V_i	Input voltage range	T_{amb}= T_{min} to T_{max}	±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C $R_L \geqslant 2\ k\Omega$ V_s= ±15V V_o= ±10V	94	106		94			86	106		dB
		T_{amb}= T_{min} to T_{max} $R_L \geqslant 2\ k\Omega$										
		V_s= ±15V V_o= ±10V	88			90			84			dB
		V_s= ±5V V_o= ±2V				80						
V_o	Output voltage swing	V_s= ±15V										
		$R_L \geqslant 10\ k\Omega$	±12	±14		±12	±14		±12	±14		V
		$R_L \geqslant 2\ k\Omega$	±10	±13		±10	±13		±10	±13		V
I_{sc}	Output short circuit current	T_{amb}= 25°C		25		10	25	35		25		mA
		T_{amb}= T_{min} to T_{max}				10		40				mA
CMR	Common mode rejection	V_s = ±20V $R_g \leqslant 10\ k\Omega$ V_{CM}=±12V	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	$R_g \leqslant 50\Omega$ V_s=±5 to ±20V				86	96					dB
		$R_g \leqslant 10k\Omega$ V_s=±5 to ±15V	77	96					77	96		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LS 141			LS 141A			LS 141C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain) Rise time Overshoot	T_{amb}= 25°C		 0.3 5			 0.25 6	 0.8 20		 0.3 5		 µs %
B	Bandwidth	T_{amb}= 25°C				0.437	1.5					MHz
SR	Slew rate	T_{amb}= 25°C		0.5		0.3	0.7			0.5		V/µs
I_s	Supply current	T_{amb}= 25°C		1.7	2.8					1.7	2.8	mA
P_{tot}	Power consumption	T_{amb}= 25°C V_s= ±20V V_s= ±15V		 50	 85		 80	 150		 50	 85	 mW mW
		V_s= ±20V T_{amb}= T_{min} T_{amb}= T_{max}						 165 135				 mW mW
		V_s= ±15V T_{amb}= T_{min} T_{amb}= T_{max}		 60 45	 100 75							 mW mW

Note: These specifications, unless otherwise specified, apply for V_s= ±15V and T_{amb}= -55 to 125°C for LS 141 and LS 141A. For the LS 141C these specifications apply for T_{amb}= 0 to 70°C

Fig. 1 - Open loop voltage gain vs. supply voltage

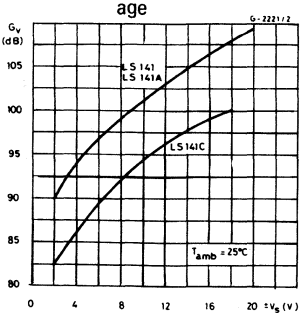


Fig. 2 - Output voltage swing vs. supply voltage

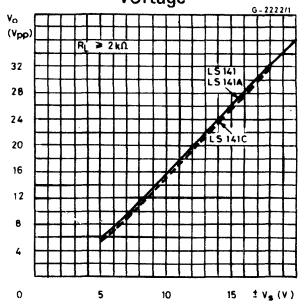


Fig. 3 - Power consumption vs. supply voltage

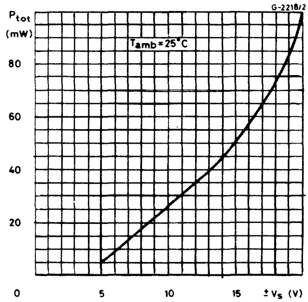


Fig. 4 - Open loop voltage gain vs. frequency

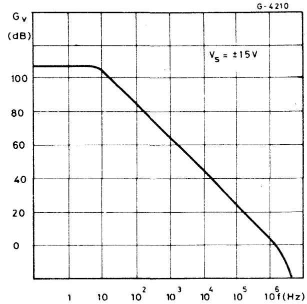


Fig. 5 - Open loop phase response vs. frequency

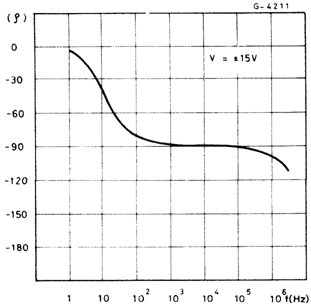


Fig. 6 - Input offset current vs. supply voltage (for LS 141 and LS 141C)

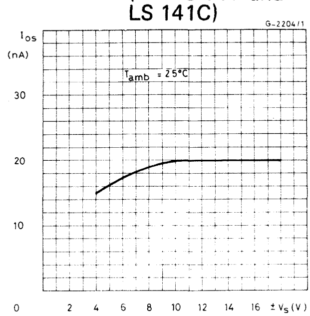


Fig. 7 - Input resistance and capacitance vs. frequency (for LS 141 and LS 141C)

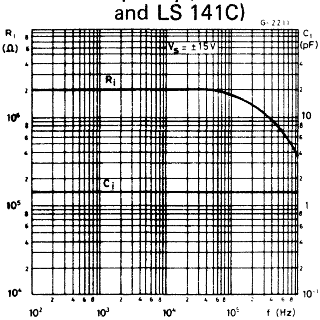


Fig. 8 - Output resistance vs. frequency

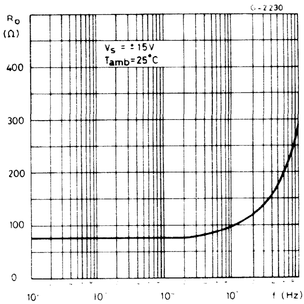


Fig. 9 - Output voltage swing vs. load resistance

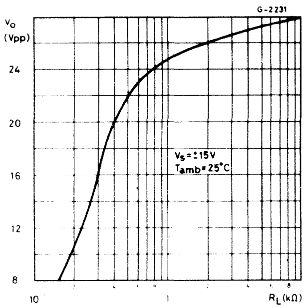


Fig. 10 - Output voltage swing vs. frequency

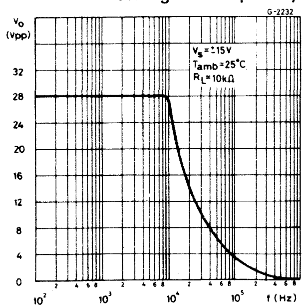


Fig. 11 - Input noise voltage vs. frequency

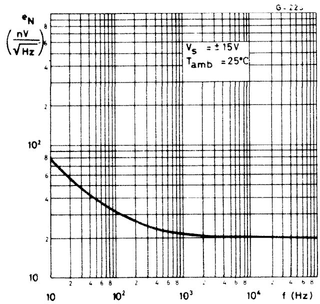


Fig. 12 - Input noise current vs. frequency

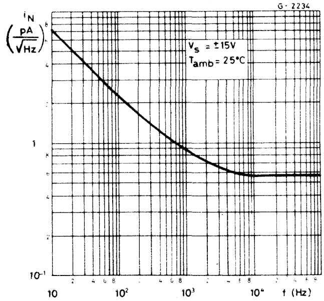


Fig. 13 - Transient response

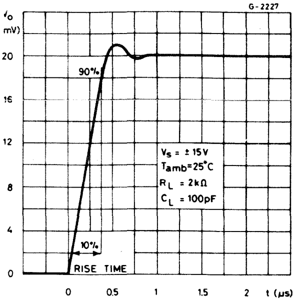


Fig. 14 - Common mode rejection ratio vs. frequency

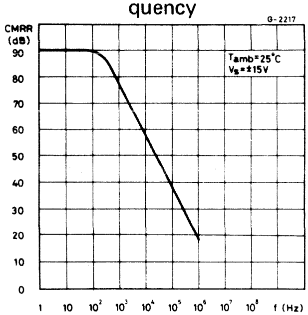
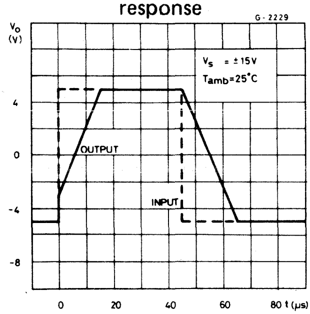


Fig. 15 - Voltage follower large signal pulse response



Typical performance curves for LS 141 and LS 141A

Fig. 16 - Input bias current vs. ambient temperature

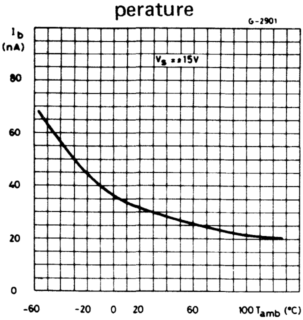


Fig. 17 - Input resistance vs. ambient temperature

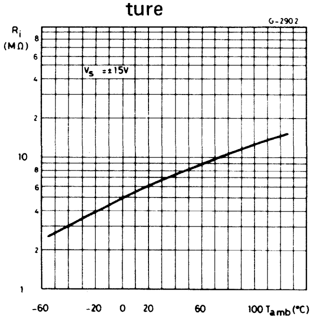


Fig. 18 - Input offset current vs. ambient temperature

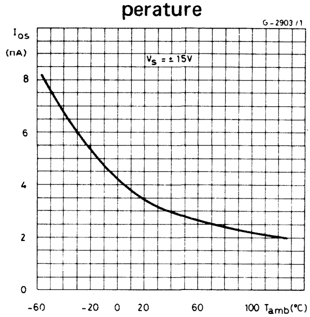


Fig. 19 - Output short-circuit current vs. ambient temperature

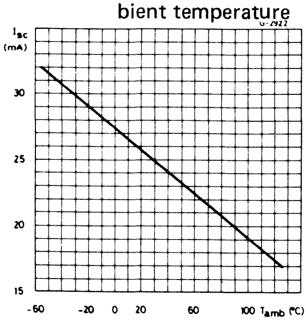


Fig. 20 - Power consumption vs. ambient temperature

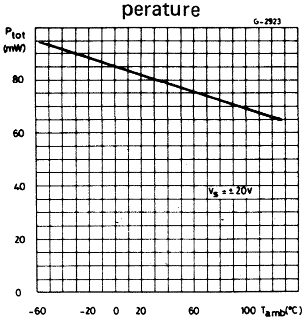
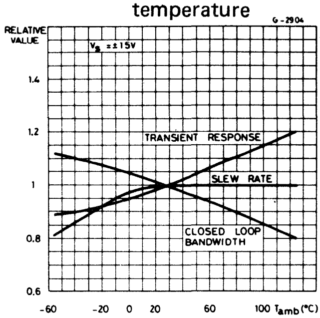


Fig. 21 - Frequency characteristics vs. ambient temperature



Typical performance curves for LS 141C

Fig. 22 - Input bias current vs. ambient temperature

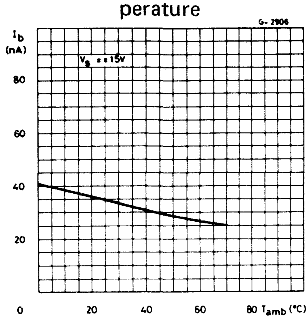


Fig. 23 - Input resistance vs. ambient temperature

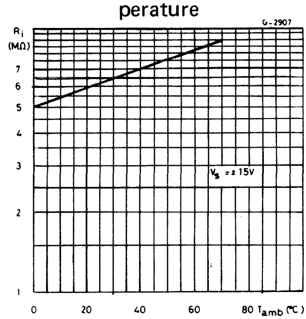


Fig. 24 - Input offset current vs. ambient temperature

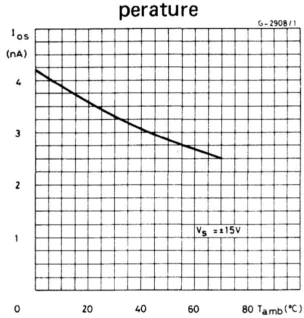


Fig. 25 - Output short circuit current vs. ambient temperature

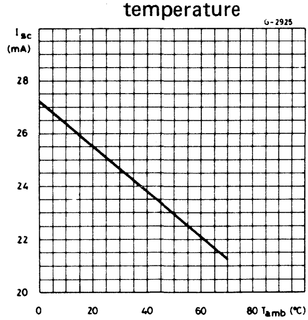


Fig. 26 - Power consumption vs. ambient temperature

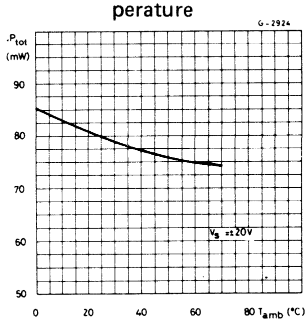
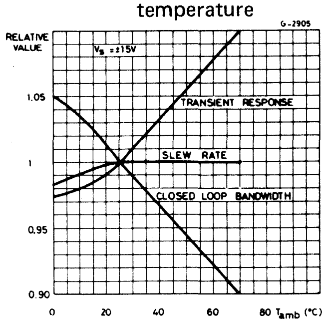


Fig. 27 - Frequency characteristics vs. ambient temperature



TYPICAL APPLICATIONS

Fig. 28 - Clipping amplifier

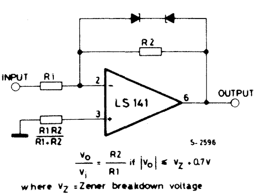


Fig. 29 - Simple integrator

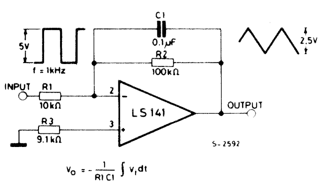
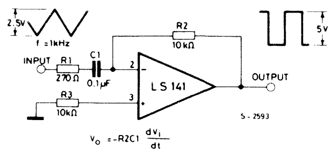


Fig. 30 - Simple differentiator



LINEAR INTEGRATED CIRCUITS

LS148
LS148A
LS148C

OPERATIONAL AMPLIFIERS

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP
- SLEW-RATE = 5.5V/μs (G_v = 10, C_C = 3.5 pF)

The LS 148 series consists of general purpose operational amplifiers, intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "Latch-up" tendencies make the LS 148 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers and general feedback applications. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. The LS 148 series is available with hermetic gold chip (8000 series). This is particularly suitable for professional and telecom applications, wherever very high MTBF are required.

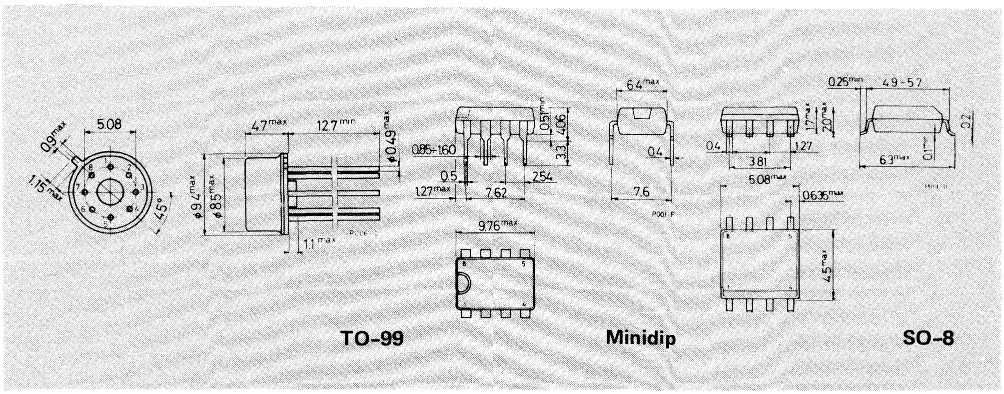
ABSOLUTE MAXIMUM RATINGS

		TO-99	Minidip	μpackage
V_s	Supply voltage		± 22V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
T_{op}	Operating temperature for **LS 148/LS 148A**		-55 to 125 °C	
	for **LS 148C**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70°C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C

1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation.

MECHANICAL DATA

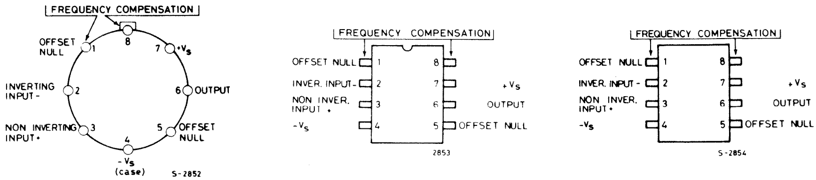
Dimensions in mm



LS148
LS148A
LS148C

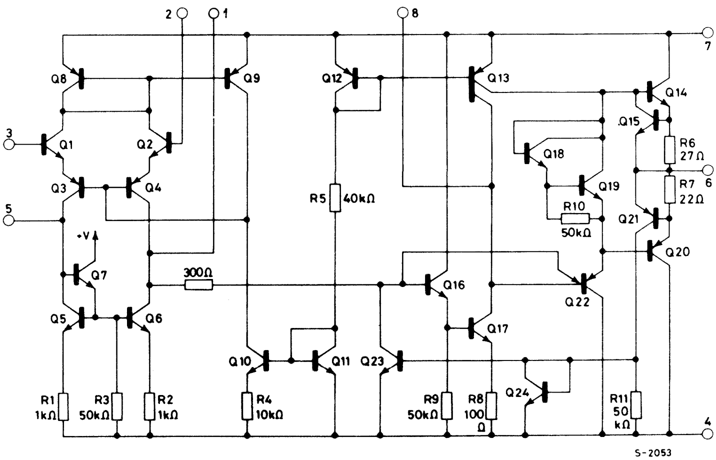
CONNECTION DIAGRAMS AND ORDERING NUMBERS

(top views)



Type	TO-99	Minidip	SO-8
LS 148	LS 148 TB	–	–
LS 148A	LS 148 ATB	–	–
LS 148C	LS 148 CTB	LS 148 CB	LS 148 CM
LS 8148	–	–	LS 8148M
LS 8148A	–	–	LS 8148 AM
LS 8148C	–	–	LS 8148 CM

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm)

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 148			LS 148A			LS 148C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C										
		$R_g \leqslant 10$ kΩ		1	5					2	6	mV
		$R_g \leqslant 50\Omega$					0.5	2				mV
		T_{amb}= T_{min} to T_{max}										
		$R_g \leqslant 10$ kΩ		1	6						7.5	mV
		$R_g \leqslant 50\Omega$					0.5	3				mV
ΔV_{os}	Input offset voltage adjust. range	T_{amb}= 25°C		±15			±25			±15		mV
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift	$R_g \leqslant 50\Omega$					2.5	15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb}= 25°C		20	200		2	10		20	200	nA
		T_{amb}= T_{min} to T_{max}		50	500			25			300	nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.15				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb}= 25°C		80	500		20	75		80	500	nA
		T_{amb}= T_{min} to T_{max}			1.5			0.1			0.8	µA
R_i	Input resistance	T_{amb}= 25°C	0.3	2		2	10		0.3	2		MΩ
V_i	Input voltage range		±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C, $R_L \geqslant 2$ kΩ, V_s= ±15V V_o= ±10V	94	104		94	108		86	104		dB
		T_{amb}= T_{min} to T_{max}, $R_L \geqslant 2$ kΩ, V_s= ±15V V_o= ±10V	88			88			84			dB
V_o	Output voltage swing	V_s= ±15V										
		$R_L \geqslant 10$ kΩ	±12	±14		±12	±14		±12	±14		V
		$R_L \geqslant 2$ kΩ	±10	±13		±10	±13		±10	±13		V
I_{sc}	Output short circuit current			25			25			25		mA
CMR	Common mode rejection	$R_g \leqslant 10$ kΩ V_{CM}= ±12V	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	V_s= ±5 to ± 20V, $R_g \leqslant 10$ kΩ	76	90		80	97		76	90		dB
SR	Slew rate	T_{amb}= 25°C, $R_L \geqslant 2$ kΩ, G_v= 1		0.5			0.5			0.5		V/µs
		T_{amb}= 25°C, $R_L \geqslant 2$ kΩ, G_v= 10*		5.5			5.5			5.5		V/µs

* C_C = 3.5 pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LS 148			LS 148A			LS 148C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain)	T_{amb}= 25°C V_i= 20 mV C_c= 30 pF R_L= 2 kΩ $C_L \leq$ 100 pF										
	Rise time			0.2			0.2			0.2		μs
	Overshoot			5			5			5		%
I_s	Supply current	T_{amb}= 25°C		1.9	2.8		1.9	2.8		1.9	2.8	mA
P_S	Power consumption	T_{amb}= 25°C V_s= ±20V					60	85				mW
		V_s= ±15V		60	85					60	85	mW
		V_s= ±15V T_{amb}= T_{min}		60	100		60	100		60	100	mW
		T_{amb}= T_{max}		45	75		40	75				mW

Note: These specifications, unless otherwise specified, apply for V_s= ±15V and T_{amb}= –55 to 125°C for LS 148 and LS 148A. For LS 148C these specifications apply for T_{amb}= 0 to 70°C (C_c= 30 pF).

Fig. 1 – Voltage offset null circuit

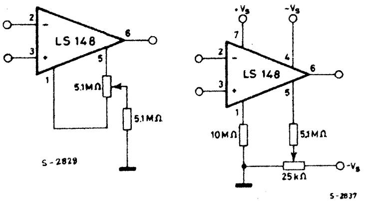
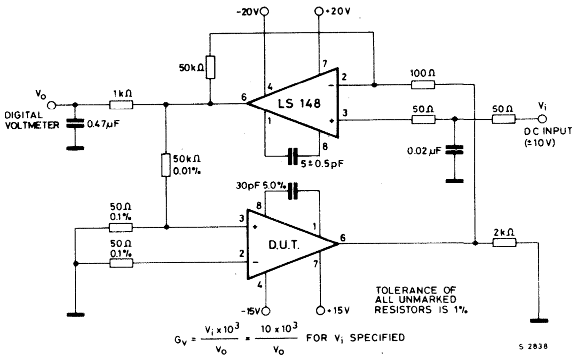


Fig. 2 – Gain test circuit



Typical performance curves for LS 148

Fig. 3 - Input bias current vs. ambient temperature

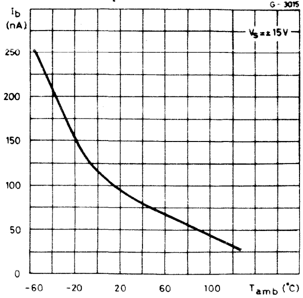


Fig. 4 - Input resistance vs. ambient temperature

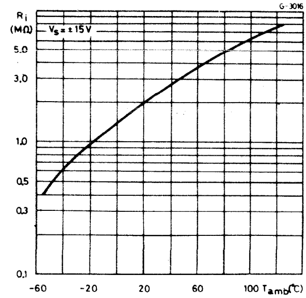


Fig. 5 - Output short-circuit current vs. ambient temperature

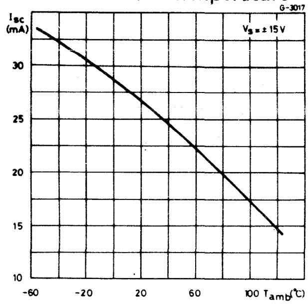


Fig. 6 - Input offset current vs. ambient temperature

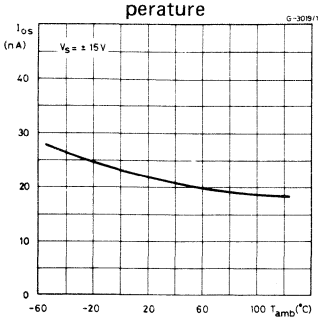


Fig. 7 - Power consumption vs. ambient temperature

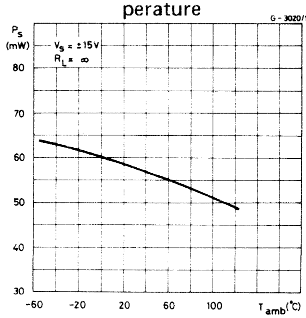
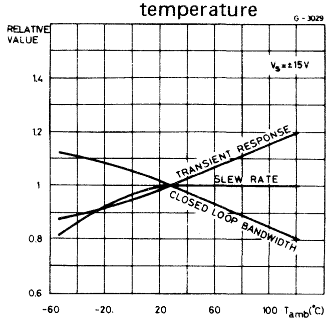


Fig. 8 - Frequency characteristics vs. ambient temperature



Typical performance curves for LS 148C

Fig. 9 - Input bias current vs. ambient temperature

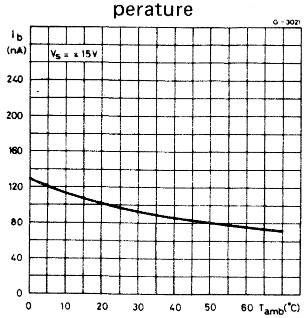


Fig. 10 - Input resistance vs. ambient temperature

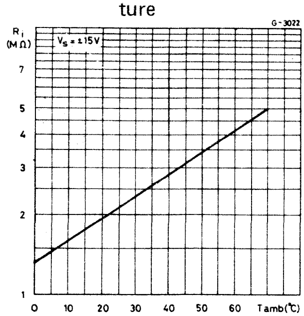


Fig. 11 - Output short-circuit current vs. ambient temperature

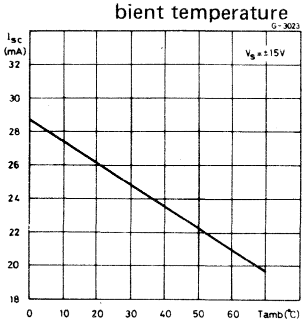


Fig. 12 - Input offset current vs. ambient temperature

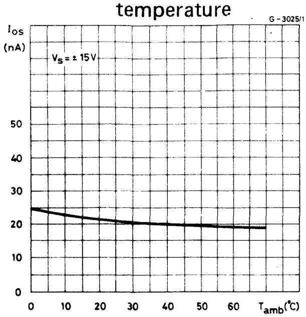


Fig. 13 - Power consumption vs. ambient temperature

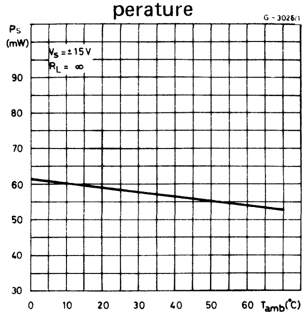
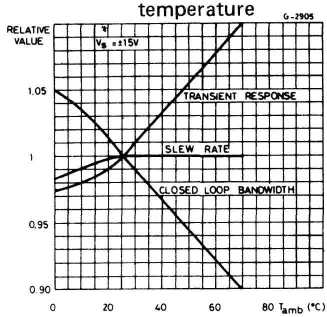


Fig. 14 - Frequency characteristics vs. ambient temperature



Typical performance curves for LS 148 and LS 148C

Fig. 15 - Open loop voltage gain vs. supply voltage

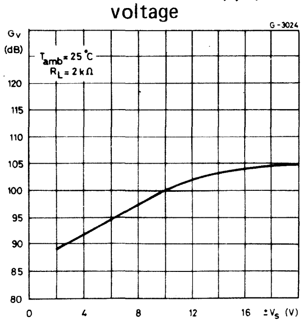


Fig. 16 - Output voltage swing vs. supply voltage

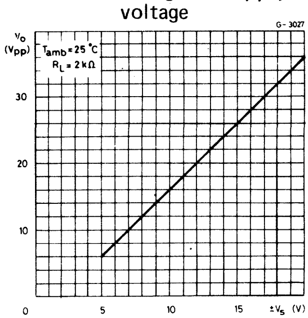


Fig. 17 - Power consumption vs. supply voltage

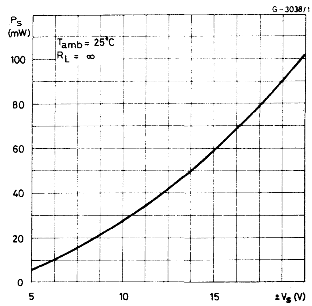


Fig. 18 - Output voltage swing vs. load resistance

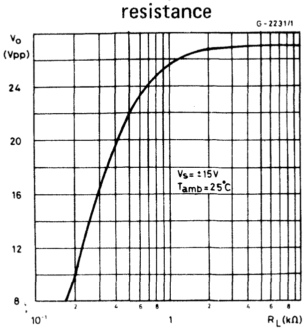


Fig. 19 - Input offset current vs. supply voltage

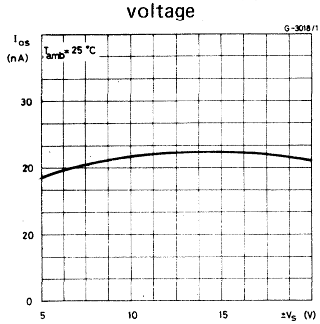


Fig. 20 - Input common mode voltage range vs. supply voltage

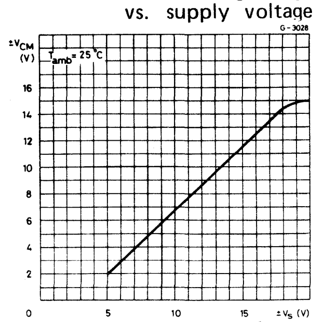


Fig. 21 - Input noise voltage vs. frequency

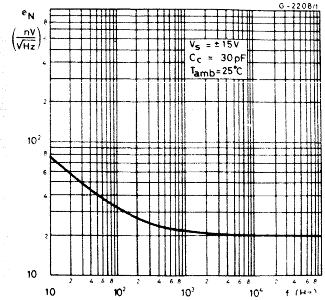


Fig. 22 - Input noise current vs. frequency

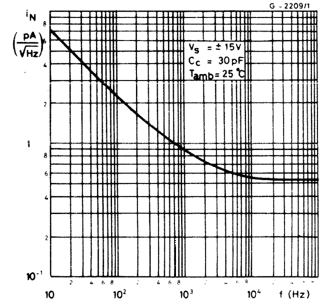


Fig. 23 - Broadband noise for various bandwidths

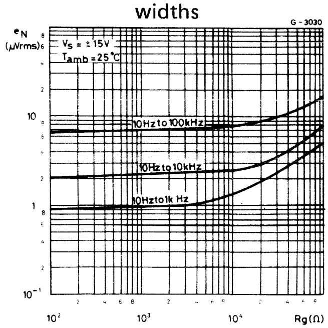


Fig. 24 - Open loop frequency and phase response vs. frequency

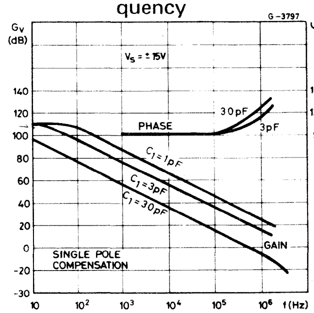


Fig. 25 - Output voltage swing vs. frequency

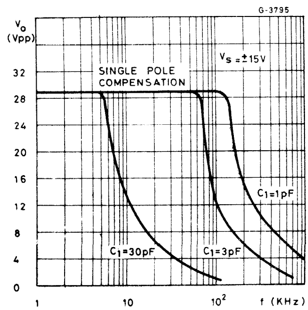


Fig. 26 - Slew-rate

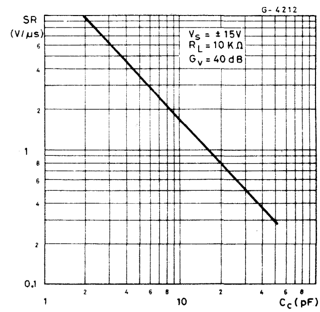


Fig. 27 - Compensation capacitance vs. closed loop voltage gain

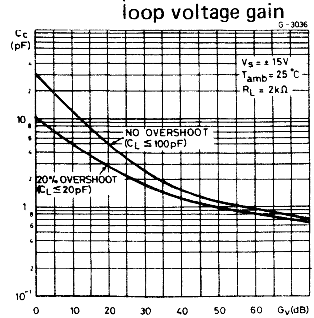


Fig. 28 - Input resistance and input capacitance vs. frequency

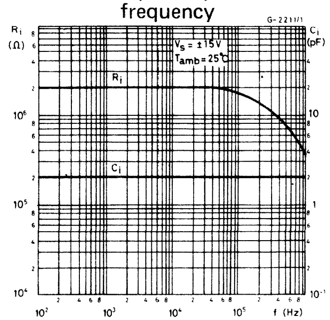


Fig. 29 - Output resistance vs. frequency

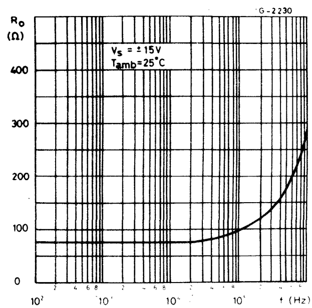


Fig. 30 - Frequency characteristics vs. supply voltage

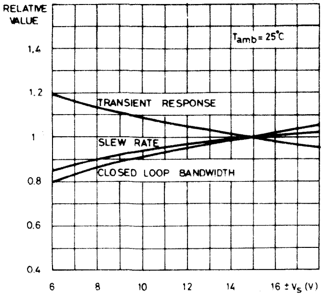


Fig. 31 - Voltage follower transient response (unity gain)

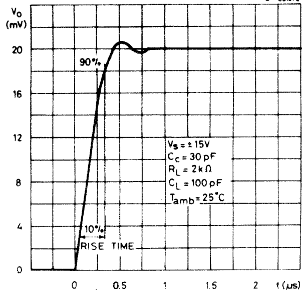


Fig. 32 - Transient response test circuit

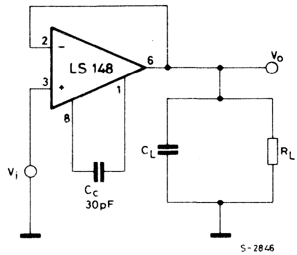


Fig. 33 - Voltage follower large-signal pulse response

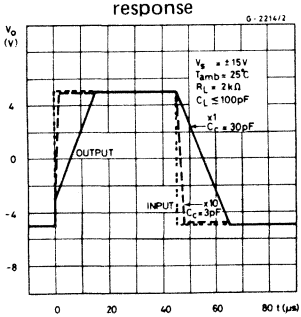


Fig. 34 - Feed forward compensation

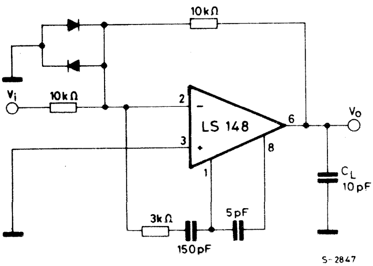
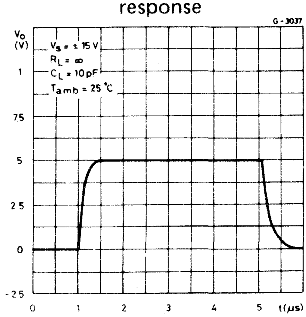
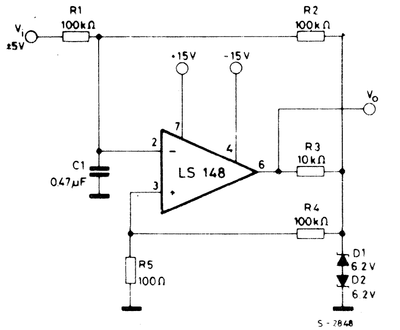


Fig. 35 - Large signal feed forward transient response



TYPICAL APPLICATIONS

Fig. 36 - Pulse width modulator



$$f_c = \frac{1}{2\pi R2\, C1}$$

$$f_n = \frac{1}{2\pi R1\, C1} = \frac{1}{2\pi R2\, C2}$$

$f_c < f_n < f_{unity\ gain}$

LINEAR INTEGRATED CIRCUITS

LS 204
LS 204A
LS 204C

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

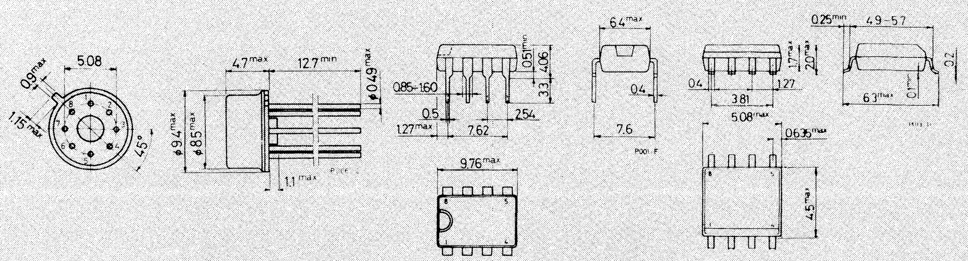
The LS 204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.). The LS 204 series is available with hermetic gold chip (8000 series).

ABSOLUTE MAXIMUM RATINGS

		TO-99	Minidip	μpackage
V_s	Supply voltage		± 18V	
V_i	Input voltage		± V_s	
V_i	Differential input voltage		± (V_s – 1)	
T_{op}	Operating temperature for **LS 204**		-25 to 85°C	
	LS 204A		-55 to 125°C	
	LS 204C		0 to 70 °C	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	665 mW	400 mW
T_j	Junction temperature	150°C	150°C	150°C
T_{stg}	Storage temperature	-65 to 150°C	-55 to 150°C	-55 to 150°C

MECHANICAL DATA

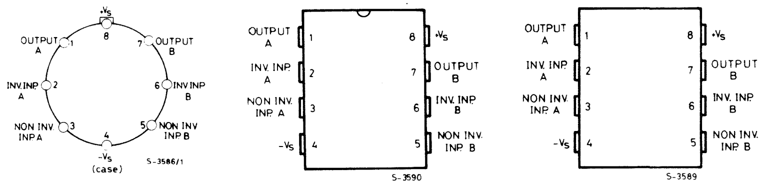
Dimensions in mm



TO-99 **Minidip** **SO-8**

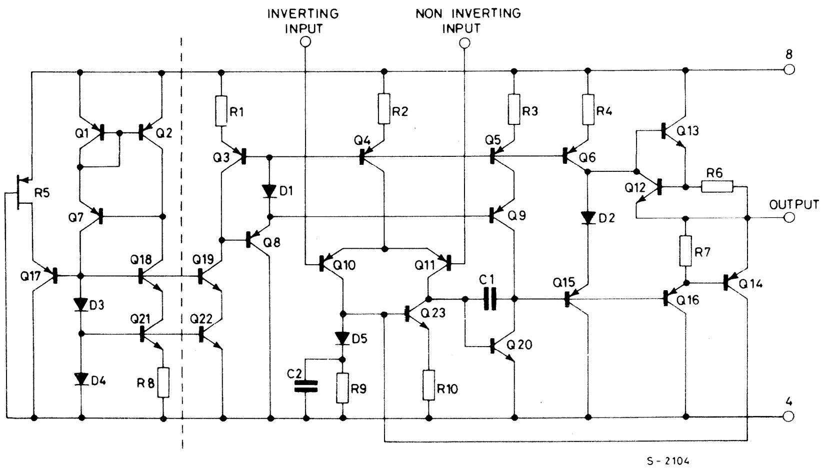
LS204
LS204A
LS204C

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



Type	TO-99	Minidip	SO-8
LS 204	LS 204 TB	—	LS 204 M
LS 204 A	LS 204 ATB	—	—
LS 204 C	LS 204 CTB	LS 204 CB	LS 204 CM
LS 8204	—	—	LS 8204 M
LS 8204 A	—	—	LS 8204 AM
LS 8204 C	—	—	LS 8204 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

		TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$ Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25x16x96 mm)

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

	Parameter	Test conditions	LS 204/LS204A Min.	LS 204/LS204A Typ.	LS 204/LS204A Max.	LS 204C Min.	LS 204C Typ.	LS 204C Max.	Unit
I_s	Supply current			0.7	1		0.8	1.5	mA
i_b	Input bias current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input resistance	f = 1 KHz		1			0.5		MΩ
V_{os}	Input offset voltage	$R_g \leqslant 10$ KΩ		0.5	2.5		0.5	3.5	mV
		$R_g \leqslant 10$ KΩ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$		5			5		µV/°C
I_{os}	Input offset current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	$T_{min} < T_{op} < T_{max}$ R_L= 2KΩ V_s= ±15V V_s= ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20 KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1 KHz R_g = 50Ω R_g = 1 KΩ R_g = 10 KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	G_v= 20 dB R_L= 2KΩ V_o= 2 Vpp f = 1 KHz		0.03	0.1		0.03	0.1	%
V_o	DC output voltage swing	R_L= 2KΩ V_s= ±15V V_s= ± 4V	±13	±3		±13	±3		V
V_o	Large signal voltage swing	R_L= 10 KΩ f = 10 KHz		28			28		Vpp
SR	Slew rate	unity gain R_L= 2KΩ	0.8	1.5			1		V/µs
CMR	Common mode rejection	V_i= 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply voltage rejection	V_i= 1V f = 100 Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel separation	f = 1 KHz	100	120			120		dB

Note:

	LS 204	LS 204A	LS 204C
$T_{min.}$	-25°C	-55°C	0°C
$T_{max.}$	+85°C	+125°C	+70°C

Fig. 1 - Supply current vs. supply voltage

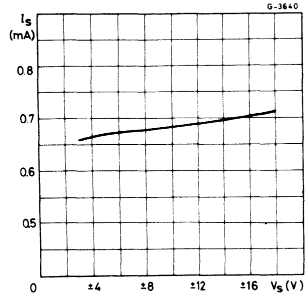


Fig. 2 - Supply current vs. ambient temperature

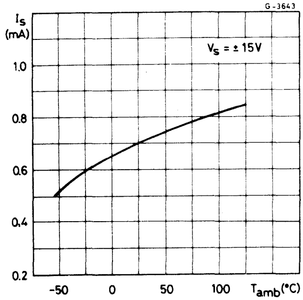


Fig. 3 - Output short circuit current vs. ambient temperature

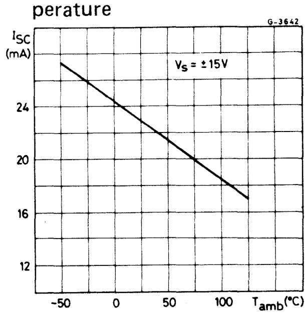


Fig. 4 - Open loop frequency and phase response

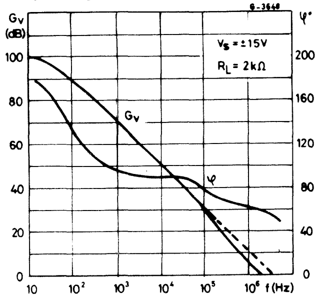


Fig. 5 - Open loop gain vs. ambient temperature

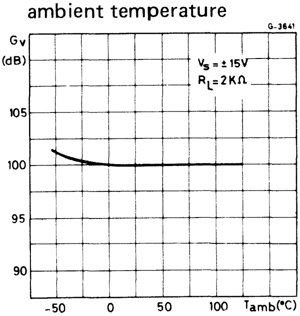


Fig. 6 - Supply voltage rejection vs. frequency

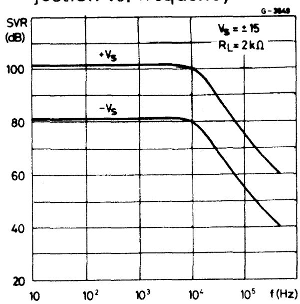


Fig. 7 - Large signal frequency response

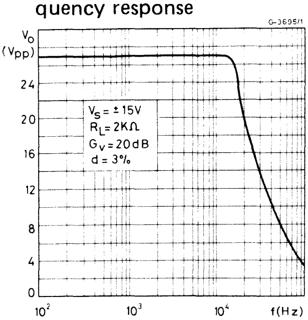


Fig. 8 - Output voltage swing vs. load resistance

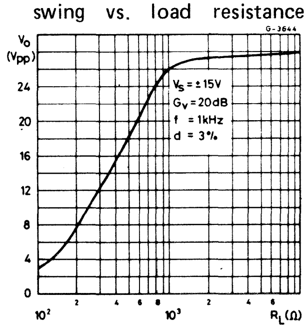
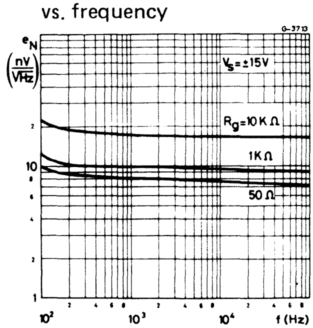


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

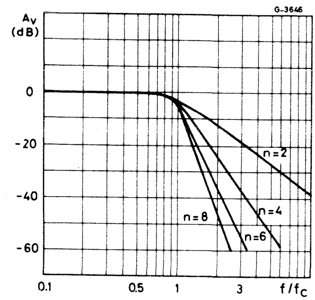
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband

Fig. 10 - Amplitude response



BESSEL

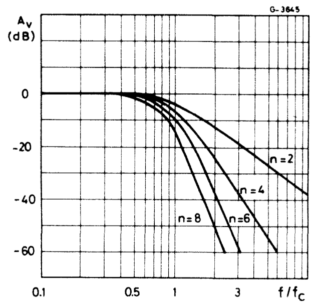
The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs
- Fast rise time.

Fig. 11 - Amplitude response

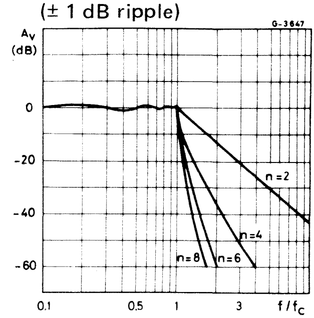


CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from ± 0.2 dB to ± 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

Fig. 12 - Amplitude response (± 1 dB ripple)



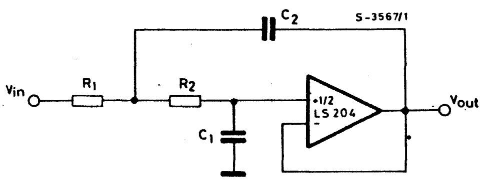
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_C$ sec.	$1.7/f_C$ sec.	$1.9/f_C$ sec.
	4	11	$1.7/f_C$	$2.8/f_C$	$3.8/f_C$
	6	14	$2.4/f_C$	$3.9/f_C$	$5.0/f_C$
	8	16	$3.1/f_C$	$5.1\ f_C$	$7.1/f_C$
BESSEL	2	0.4	$0.8/f_C$	$1.4/f_C$	$1.7/f_C$
	4	0.8	$1.0/f_C$	$1.8/f_C$	$2.4/f_C$
	6	0.6	$1.3/f_C$	$2.1/f_C$	$2.7/f_C$
	8	0.3	$1.6/f_C$	$2.3/f_C$	$3.2/f_C$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_C$	$1.6/f_C$	-
	4	18	$3.0/f_C$	$5.4/f_C$	-
	6	21	$5.9/f_C$	$10.4/f_C$	-
	8	23	$8.4/f_C$	$16.4/f_C$	-
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_C$	$2.7/f_C$	-
	4	28	$4.8/f_C$	$8.4/f_C$	-
	6	32	$8.2/f_C$	$16.3/f_C$	-
	8	34	$11.6/f_C$	$24.8/f_C$	-

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:

$\omega_c = 2\pi\ f_c$ with f_c = cutoff frequency

ξ = damping factor.

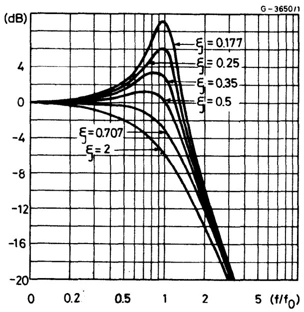
APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.
The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Tab. I

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v= -3 dB
Chebyschev	$<\frac{\sqrt{2}}{2}$	$>\frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed R= $R_1 = R_2$, we have (see fig. 13)

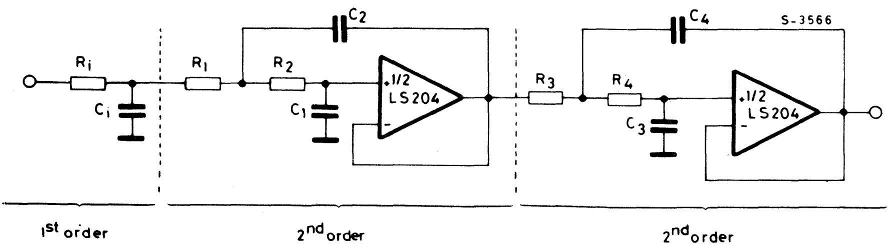
$$C_1 = \frac{1}{R}\ \frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\ \frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
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8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1\ nF$ we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

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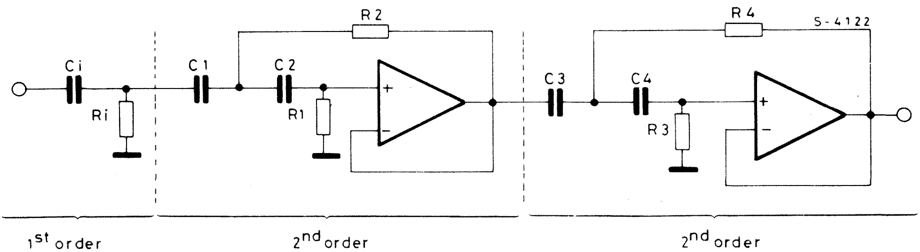
Fig. 16 - 5^{th} order high-pass filter (Butterworth) with unity gain configuration.



LINEAR INTEGRATED CIRCUITS

LS 404
LS 404C

HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

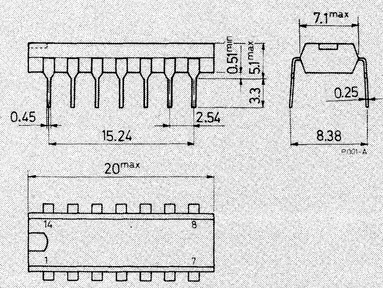
The LS 404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.).
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.
The LS 404 is available with hermetic gold chip (8000 series).

ABSOLUTE MAXIMUM RATINGS

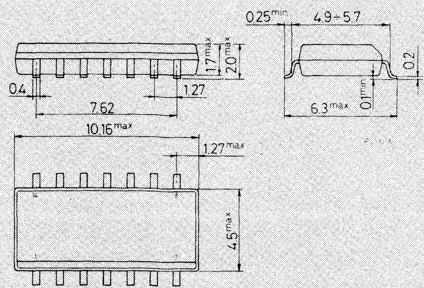
V_s	Supply voltage		± 18	V
V_i	Input voltage	(positive)	$+V_s$	
		(negative)	$-V_s - 0.5$	V
V_i	Differential input voltage		$\pm (V_s - 1)$	
T_{op}	Operating temperature	**LS 404**	-25 to + 85	°C
		LS 404C	0 to + 70	°C
P_{tot}	Power dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage temperature		-55 to + 150	°C

MECHANICAL DATA

Dimensions in mm



DIP 14

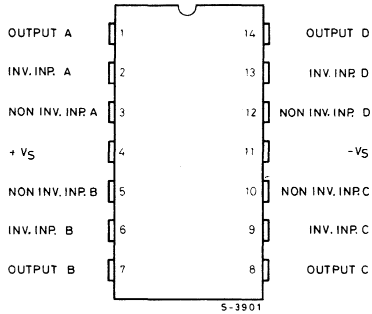


SO 14

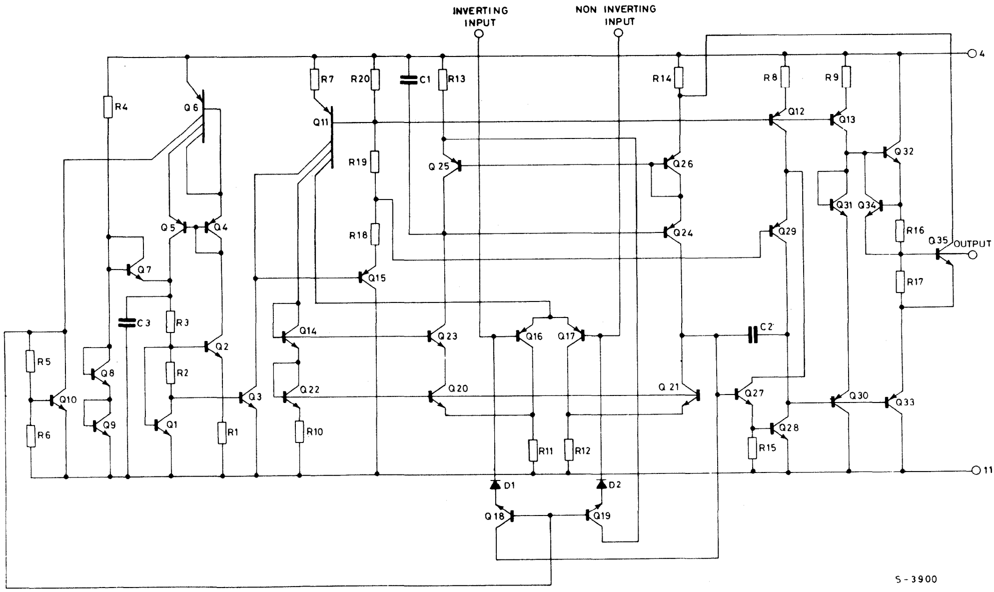
LS404
LS404C

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)

Type	DIP 14	SO-14
LS 404 LS 404C	– LS 404CB	LS 404M LS 404CM
LS 8404 LS 8404C	– –	LS 8404M LS 8404CM



SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			DIP 14	SO-14
$R_{thj-amb}$	Thermal resistance junction-ambient	max	200°C/W	200°C/W*

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm.)

ELECTRICAL CHARACTERISTICS ($V_s = \pm 12V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	LS 404			LS 404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			1.3	2		1.5	3	mA
I_b	Input bias current			50	200		100	300	nA
R_i	Input resistance	f = 1KHz		0.7			0.5		MΩ
V_{os}	Input offset voltage	R_g = 10KΩ		1	2.5		1	5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input offset current			10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	R_L = 2KΩ V_s = ±12V V_s = ±4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	unity gain R_L = 2KΩ, f = 1 KHz V_o = 2Vpp, f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC output voltage swing	R_L = 2KΩ, V_s = ± 12V V_s = ± 4V	± 10	 ± 3		± 10	 ± 3		V
V_o	Large signal voltage swing	f = 10KHz, R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		Vpp
SR	Slew rate	unity gain R_L = 2KΩ	0.8	1.5			1		V/μs
CMR	Comm. mode rejection	V_i = 10V	90	94		80	90		dB
SVR	Supply voltage rejection	V_i = 1V f = 100Hz	90	94		86	90		dB
CS	Channel separation	f = 1KHz	100	120			120		dB

Fig. 1 - Supply current vs. supply voltage

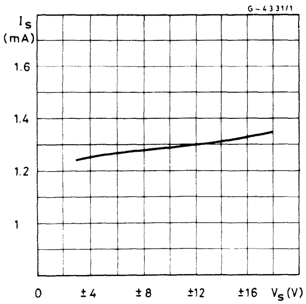


Fig. 2 - Supply current vs. ambient temperature

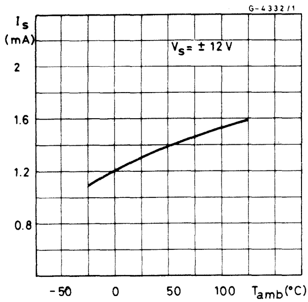


Fig. 3 - Output short circuit current vs. ambient temperature

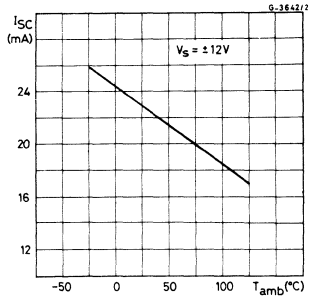


Fig. 4 - Open loop frequency and phase response

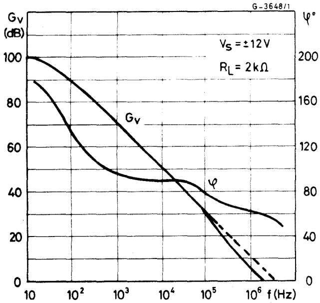


Fig. 5 - Open loop gain vs. ambient temperature

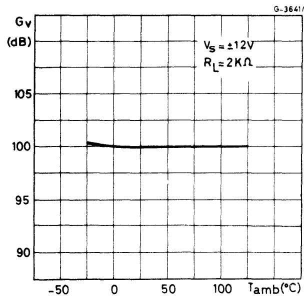


Fig. 6 - Supply voltage rejection vs. frequency

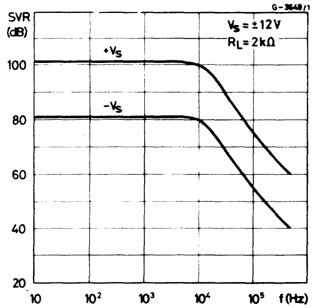


Fig. 7 - Large signal frequency response

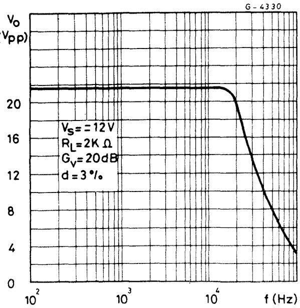


Fig. 8 - Output voltage swing vs. load resistance

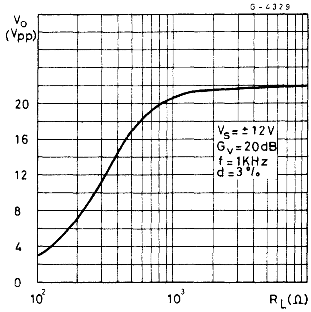
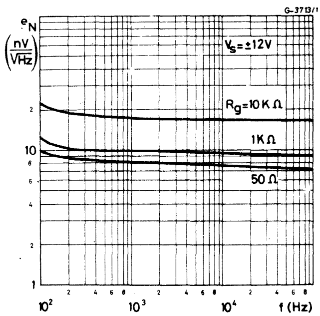


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs.

Fig. 10 - Amplitude response

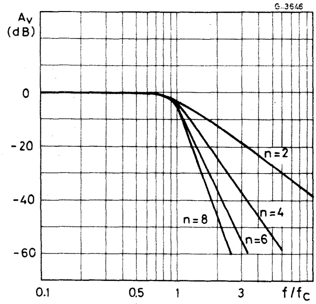


Fig. 11 - Amplitude response

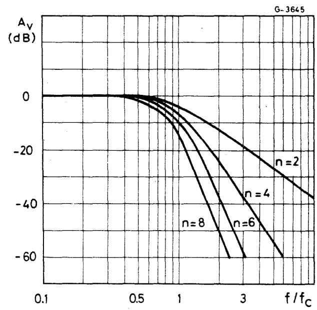
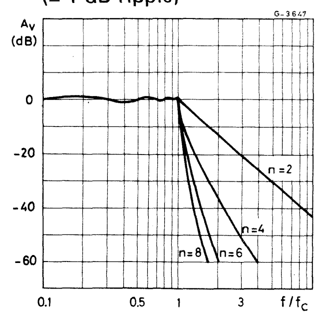


Fig. 12 - Amplitude response (± 1 dB ripple)



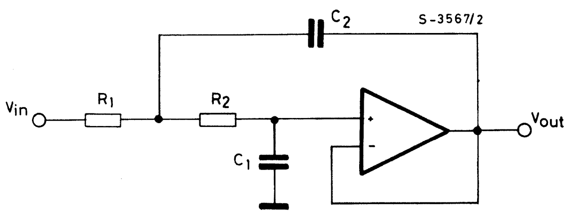
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filter to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

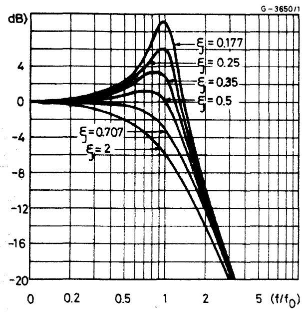
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

TAB. 1

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v = -3 dB
Chebyschev	$<\frac{\sqrt{2}}{2}$	$>\frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

$$C_1 = \frac{1}{R}\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

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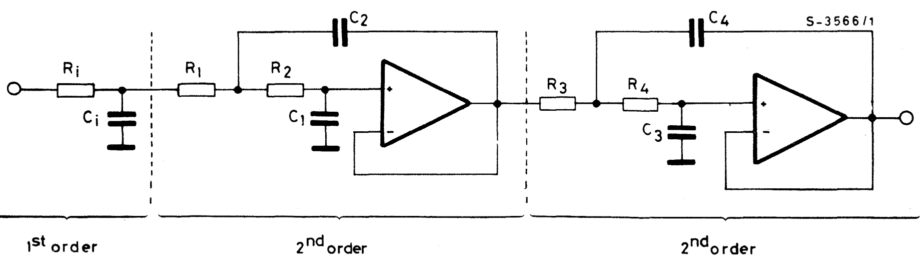

APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

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Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
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5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02·	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1\ nF$ we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

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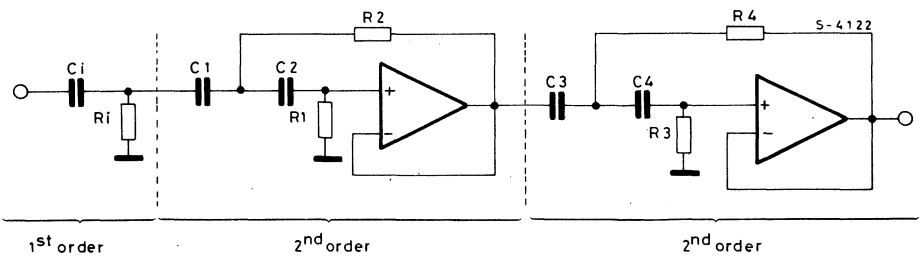
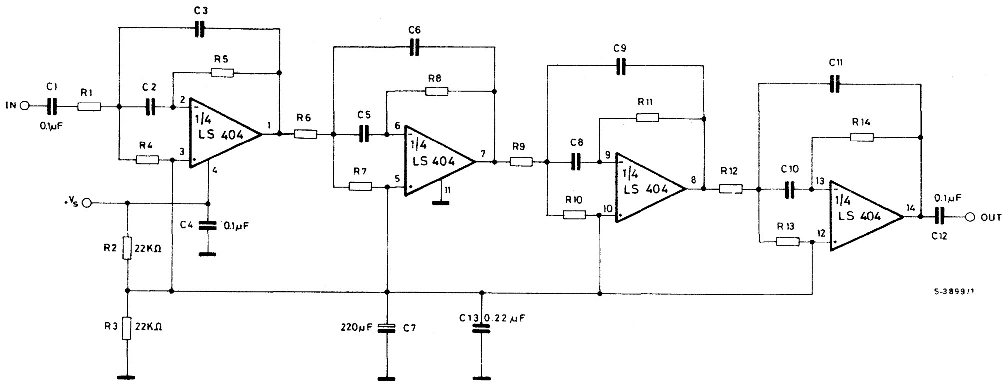
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

Fig. 17 – Multiple feedback 8-pole bandpass filter.



$f_c = 1.180Hz$; $A = 1$; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11} = 3.300\ pF$;
$R_1 = R_6 = R_9 = R_{12} = 160\ K\Omega$; $R_5 = R_8 = R_{11} = R_{14} = 330K\Omega$; $R_4 = R_7 = R_{10} = R_{13} = 5.3K\Omega$

Fig. 18 – Frequency response of band-pass filter

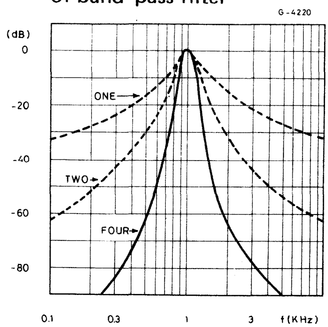
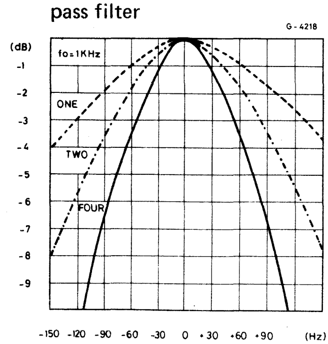
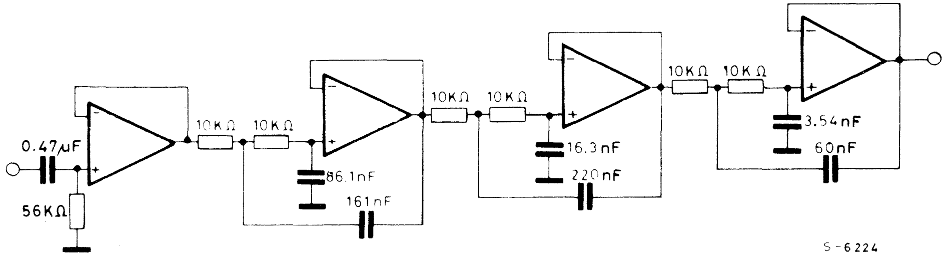


Fig. 19 – Bandwidth of band-pass filter



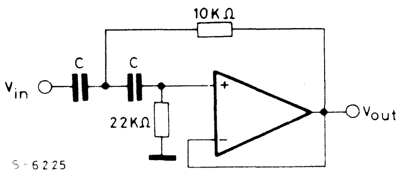
APPLICATION INFORMATION (continued)

Fig. 20 - Six-pole 355 Hz low-pass filter (Chebychev type)



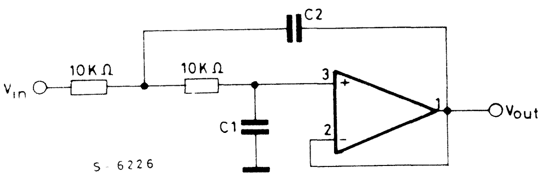
This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Fig. 21 - Subsonic filter (G_v = 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Fig. 22 - High cut filter (G_v = 0 dB)



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

LINEAR INTEGRATED CIRCUITS

LS709
LS709A
LS709C

OPERATIONAL AMPLIFIERS

The LS 709 series features low offset, high input impedance, large input common mode range, high output voltage swing. The amplifier is intended for use in D.C. servosystems, high impedance analog computer, low level instrumentation applications, and for the generation of special linear and non linear transfer functions.

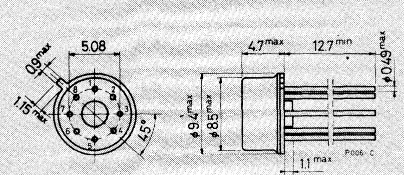
ABSOLUTE MAXIMUM RATINGS

		TO-99	DIP
V_s	Supply voltage	± 18 V	
V_i (1)	Input voltage	± 10 V	
ΔV_i	Differential input voltage	± 5 V	
T_{op}	Operating temperature for **LS 709/LS 709A**	-55 to 125 °C	
	for **LS 709C**	0 to 70 °C	
P_{tot}	Power dissipation at T_{amb} = 70 °C	520 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C

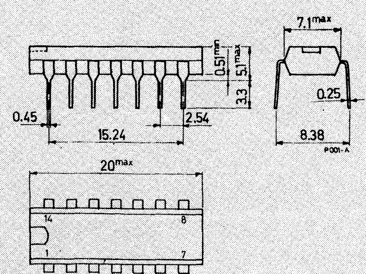
1) For supply voltages less than ± 10V maximum input voltage is equal to the supply voltage.

MECHANICAL DATA

Dimensions in mm



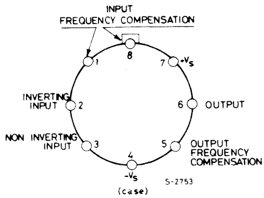
TO-99

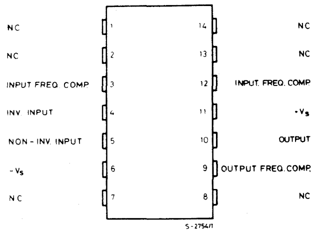


DIP

LS709
LS709A
LS709C

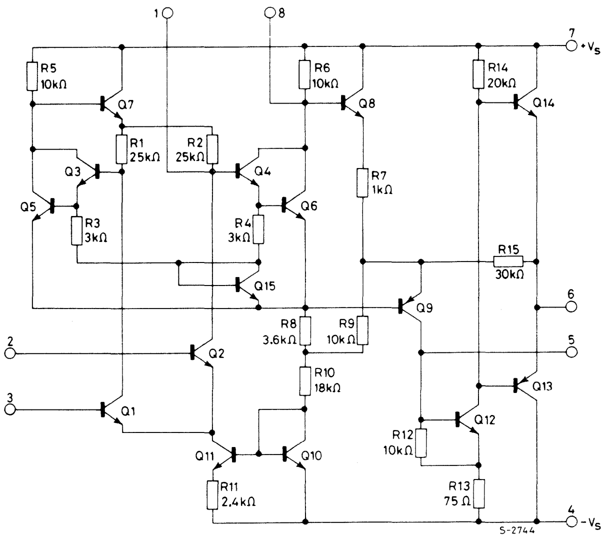
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-99	DIP
LS 709	LS 709 TB	–
LS 709A	LS 709 ATB	–
LS 709C	LS 709 CTB	LS 709 CB

SCHEMATIC DIAGRAM (pin numbers are referred to the TO-99 version)



THERMAL DATA

			TO-99	DIP
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	200 °C/W

ELECTRICAL CHARACTERISTICS (see note)

	Parameter	Test conditions	LS 709A			LS 709			LS 709C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 10\ k\Omega$ $T_{amb}=25°C$		 0.6	3 2		 1	6 5		 2	10 7.5	mV mV
I_b	Input bias current	$T_{amb}= T_{min}$ $T_{amb}= 25°C$		0.3 100	0.6 200		0.5 200	1.5 500		0.36 300	2 1500	μA nA
I_{os}	Input offset current	$T_{amb}= T_{max}$ $T_{amb}= T_{min}$ $T_{amb}= 25°C$		3.5 40 10	50 250 50		20 100 50	200 500 200		75 125 100	400 750 500	nA nA nA
R_i	Input resistance	$T_{amb}= T_{min}$ $T_{amb}= 25°C$	85 350	170 700		40 150	100 400		50 50	250 250		kΩ kΩ
R_o	Output resistance	$T_{amb}= 25°C$		150			150			150		Ω
I_s	Supply current	$V_s= \pm 15V$ $T_{amb}=25°C$		2.5	3.6		2.6	5.5		2.6	6.6	mA
	Transient response Risetime Overshoot	$V_i= 20\ mV$ $C_L \leq 100\ pF$ $T_{amb}= 25°C$			1.5 30		0.3 10	1 30		0.3 10	1 30	μs %
SR	Slew rate	$T_{amb}= 25°C$		0.25			0.25			0.25		V/μs
$\frac{\Delta V_{os}}{\Delta T}$	Average temperature coefficient of input offset voltage	$R_g= 50\Omega$ $T_{amb}= 25°C$ to T_{max} $T_{amb}= 25°C$ to T_{min} $R_g= 10\ k\Omega$ $T_{amb}= 25°C$ to T_{max} $T_{amb}= 25°C$ to T_{min}		 1.8 1.8 2 4.8	 10 10 15 25		 3 6			 6 12		 μV/°C μV/°C μV/°C μV/°C
G_v	Large signal voltage gain	$V_s= \pm 15V$ $R_L \geq 2\ k\Omega$ $V_o= \pm 10V$	88	93	97	88	93	97	83	93		dB
V_o	Output voltage swing	$V_s= \pm 15V$ $R_L= 10\ k\Omega$ $V_s= \pm 15V$ $R_L= 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
V_i	Input voltage range	$V_s= \pm 15V$	±8			±8	±10		±8	±10		V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	80	110		70	90		65	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	80	88		76	92		74	92		dB

Note: These specifications, unless otherwise specified, apply for $T_{amb}= -55$ to 125°C for LS 709/LS 709A and $T_{amb}= 0$ to 70°C for LS 709C with the following conditions: $V_s= \pm 9V$ to $\pm 15V$, C1= 5000 pF, R1= 1.5 kΩ, C2= 200 pF and R2= 51Ω. (See fig. 8 and fig. 17).

Fig. 1 - Voltage gain vs. supply voltage (for 709A)

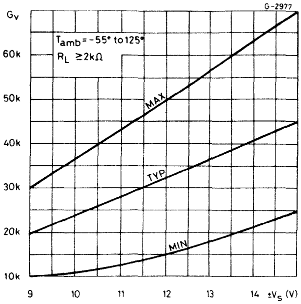


Fig. 2 - Output voltage swing vs. supply voltage (for 709A)

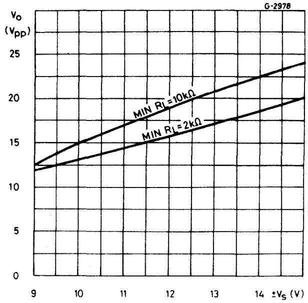


Fig. 3 - Input common mode voltage range vs. supply voltage (for 709A)

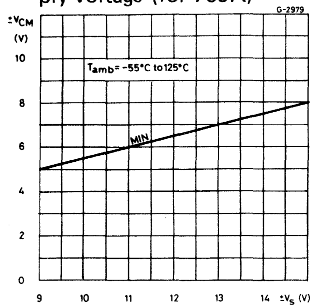


Fig. 4 - Power consumption vs. supply voltage (for 709A)

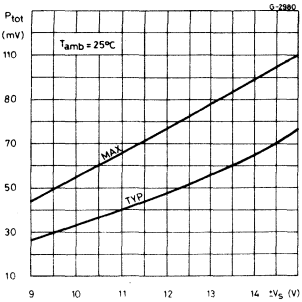


Fig. 5 - Output voltage swing vs. load resistance (for 709A)

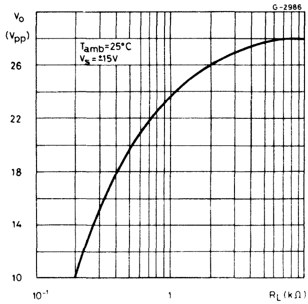


Fig. 6 - Input bias current vs. ambient temperature (for 709A)

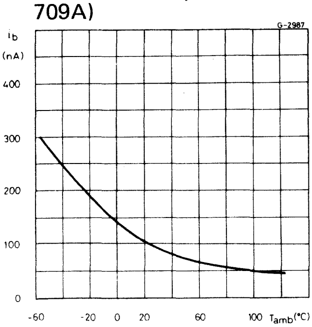


Fig. 7 - Input offset current vs. ambient temperature (for 709A)

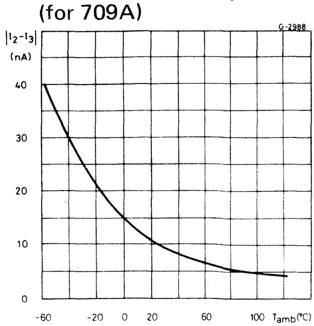


Fig. 8 - Transient response test circuit

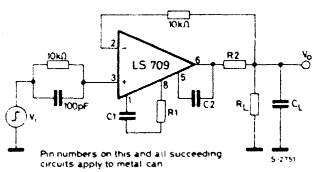


Fig. 9 - Transient response (for 709A)

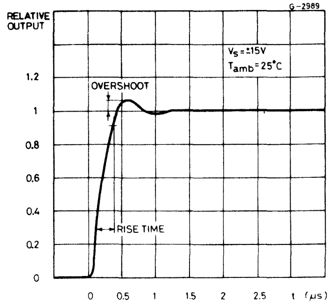


Fig. 10 - Slew rate vs. closed loop gain using recommended compensation networks (for 709A)

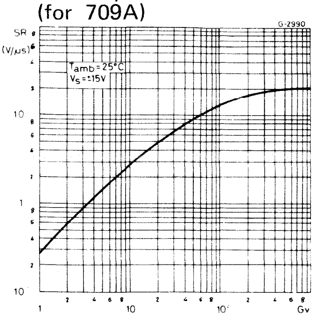


Fig. 11 - Voltage gain vs. supply voltage (for 709)

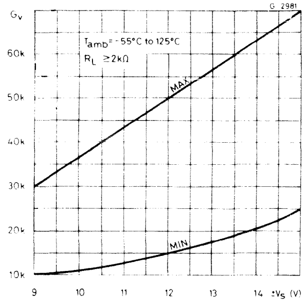


Fig. 12 - Output voltage swing vs. supply voltage (for 709 and 709C)

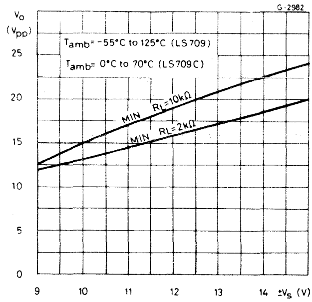


Fig. 13 - Voltage gain vs. supply voltage (for 709C)

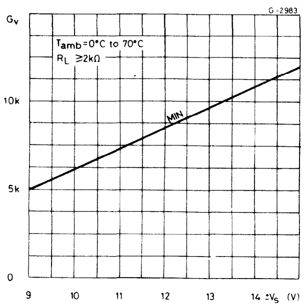


Fig. 14 - Input bias current vs. ambient temperature (for 709C)

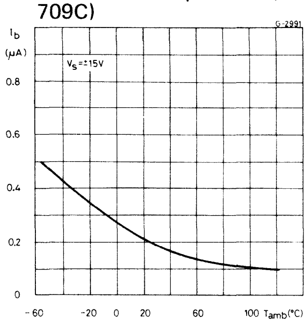
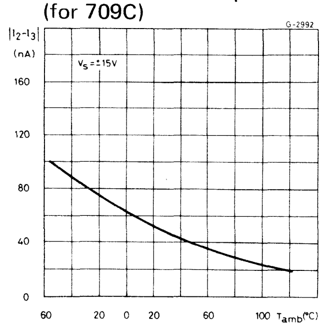


Fig. 15 - Input offset current vs. ambient temperature (for 709C)



Frequency compensation for all types

Fig. 16 - Open loop frequency response for various values of compensation

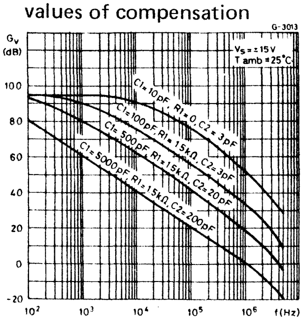


Fig. 17 - Frequency compensation circuit

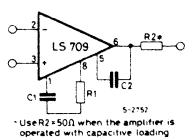
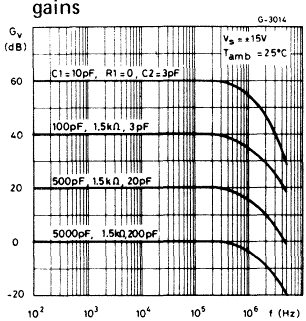


Fig. 18 - Frequency response for various closed loop gains



PROGRAMMABLE OPERATIONAL AMPLIFIER

- MICROPOWER CONSUMPTION
- INTERNALLY FREQUENCY COMPENSATION
- OFFSET NULL CAPABILITY
- SHORT CIRCUIT PROTECTION
- LOW INPUT BIAS CURRENTS
- LOW NOISE

The LS 776 is a programmable operational amplifier available in three different packages (TO-99, Minidip and SO-8 micropackage). High input impedance, low supply currents and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics, make it an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption and input current can be optimized by a single resistor of current source that sets the quiescent current for nanowatt power consumption or for characteristics similar to the LS 141. Internal frequency compensation, absence of "latch-up", high slew rate and short circuit current protection assure ease of use in long interval integrators, active filters and sample and hold circuits. The LS 776 is available with hermetic gold chip (8000 Series).

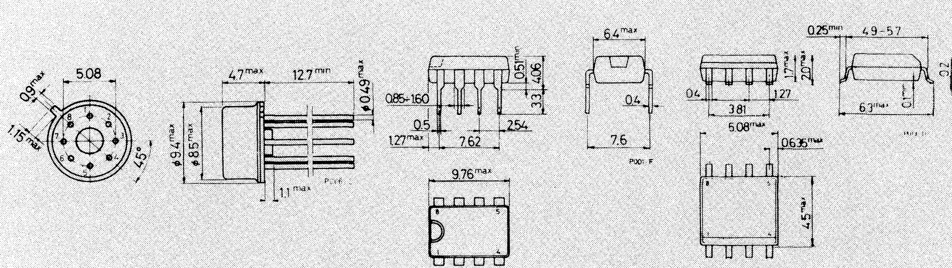
ABSOLUTE MAXIMUM RATINGS

		TO-99	Minidip	µpackage
V_s	Supply voltage		± 18V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
V_{SET}	Maximum voltage to ground at I_{SET}		V_s -2V to V_s	
I_{SET}	Maximum current at I_{SET}		500 µA	
T_{op}	Operating temperature for **LS 776**		-55 to 125 °C	
	for **LS 776 C**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70 °C	520 mW	665 mW	400 mW
T_{stg}, T_j	Storage and junction temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C

1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

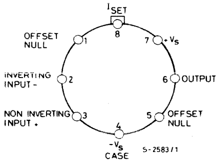
MECHANICAL DATA

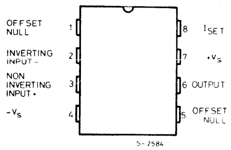
Dimensions in mm

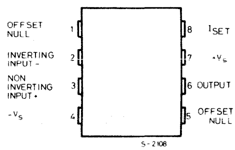


TO-99 Minidip SO-8

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

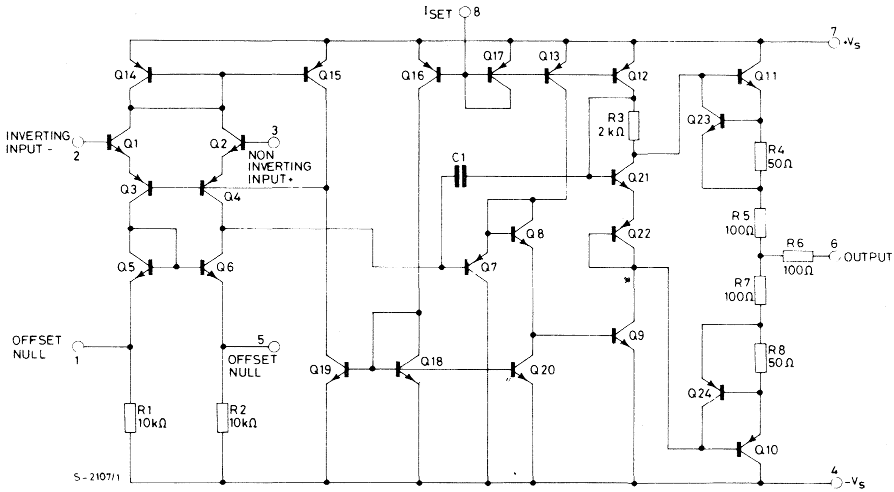






Type	TO-99	Minidip	SO-8
LS 776	LS 776 TB	–	–
LS 776C	LS 776 CTB	LS 776 CB	LS 776CM
LS 8776	–	–	LS 8776M
LS 8776C	–	–	LS 8776CM

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	155 °C/W	120 °C/W	200* °C/W

* The thermal resistance is measured with device mounted on a ceramic substrate (25 x 16 x 0.6 mm)

ELECTRICAL CHARACTERISTICS for LS 776

($V_s = \pm 15V$, $T_{amb} = 25°C$ unless otherwise specified)

Symbol	Parameter	Test conditions	$I_{SET} = 1.5\ \mu A$ Min.	$I_{SET} = 1.5\ \mu A$ Typ.	$I_{SET} = 1.5\ \mu A$ Max.	$I_{SET} = 15\ \mu A$ Min.	$I_{SET} = 15\ \mu A$ Typ.	$I_{SET} = 15\ \mu A$ Max.	Unit
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$		2	5		2	5	mV
I_{OS}	Input offset current	$R_g \leq 10\ k\Omega$		0.7	3		2	15	nA
I_b	Input bias current			2	7.5		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ $V_o = \pm 10\ V$	106	112					dB
		$R_L \geq 5\ k\Omega$ $V_o = \pm 10\ V$				100	112		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			12		mA
I_s	Supply current			20	25		160	180	μA
P_S	Power consumption				0.75			5.4	mW
	Transient response (unity gain)	$V_i = 20\ mV$ $R_L \geq 5\ k\Omega$ $C_L = 100\ pF$							
	Rise time t_r			1.6			0.35		μs
	Overshoot ΔV_o			0			10		%
SR	Slew rate	$R_L \geq 5\ k\Omega$		0.1			0.8		V/μs
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 12	± 14					V
		$R_L \geq 5\ k\Omega$				± 10	± 13		V
The following specifications apply for $T_{amb} = -55$ to $125\ °C$									
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$			6			6	mV
I_{OS}	Input offset current	$T_{amb} = 125°C$			5			15	nA
		$T_{amb} = -55°C$			10			40	nA
I_b	Input bias current	$T_{amb} = 125°C$			7.5			50	nA
		$T_{amb} = -55°C$			20			120	nA
V_i	Input voltage range		± 10			± 10			V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	90		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	76	92		76	92		dB
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ $V_o = \pm 10V$	100			98			dB
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 10			± 10			V
I_s	Supply current				30			200	μA
P_S	Power consumption				0.9			6	mW

ELECTRICAL CHARACTERISTICS for LS 776
(V_s= ± 3V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	R_g ⩽ 10 kΩ		2	5		2	5	mV
I_{OS}	Input offset current			0.7	3		2	15	nA
I_b	Input bias current			2	7.5		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	R_L ⩾ 75 kΩ V_o= ± 1V	94	106					dB
		R_L ⩾ 5 kΩ V_o= ± 1V				94	106		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			5		mA
I_s	Supply current			13	20		130	160	μA
P_S	Power consumption			78	120		780	960	μW
	Transient response (unity gain)	V_i = 20 m V R_L ⩾ 5 kΩ C_L ⩽ 100 pF							
	Rise time t_r			3			0.6		μs
	Overshoot ΔV_o			0			5		%
SR	Slew rate	R_L ⩾ 5 kΩ		0.03			0.35		V/μs
The following specifications apply for T_{amb}= -55 to 125°C									
V_{OS}	Input offset voltage	R_g ⩽ 10 kΩ			6			6	mV
I_{OS}	Input offset current	T_{amb}= 125°C			5			15	nA
		T_{amb}= -55°C			10			40	nA
I_b	Input bias current	T_{amb}= 125°C			7.5			50	nA
		T_{amb}= -55°C			20			120	nA
V_i	Input voltage range		± 1			± 1			V
CMR	Common mode rejection	R_g ⩽ 10 kΩ	70	86		70	86		dB
SVR	Supply voltage rejection	R_g ⩽ 10 kΩ	76	92		76	92		dB
G_v	Large signal voltage gain	R_L ⩾ 75 kΩ V_o= ± 1V	88						dB
		R_L ⩾ 5 kΩ V_o= ± 1V				88			dB
V_o	Output voltage swing	R_L ⩾ 75 kΩ	± 2	± 2.4					V
		R_L ⩾ 5 kΩ				± 1.9	± 2.1		V
I_s	Supply current				25			180	μA
P_S	Power consumption				150			1080	μW

ELECTRICAL CHARACTERISTICS for LS 776C

($V_s = \pm$ 15V, $T_{amb} = 25°C$ unless otherwise specified)

	Parameter	Test conditions	$I_{SET} = 1.5\ \mu A$			$I_{SET} = 15\ \mu A$			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$		2	6		2	6	mV
I_{OS}	Input offset current			0.7	6		2	25	nA
I_b	Input bias current			2	10		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ $V_o = \pm 10V$	94	112					dB
		$R_L \geq 5\ k\Omega$ $V_o = \pm 10V$				94	112		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			12		mA
I_s	Supply current			20	30		160	190	μA
P_S	Power consumption				0.9			5.7	mW
	Transient response (unity gain)	$V_i = 20\ mV$ $R_L \geq 5\ k\Omega$ $C_L \leq 100\ pF$							
	Rise time t_r			1.6			0.35		μs
	Overshoot ΔV_o			0			10		%
SR	Slew rate	$R_L \geq 5\ k\Omega$		0.1			0.8		V/μs
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 12	± 14					V
		$R_L \geq 5\ k\Omega$				± 10	± 13		V
The following specifications apply for $T_{amb} = 0$ to 70°C									
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$			7.5			7.5	mV
I_{OS}	Input offset current	$T_{amb} = 70°C$			6			25	nA
		$T_{amb} = 0°C$			10			40	nA
I_b	Input bias current	$T_{amb} = 70°C$			10			50	nA
		$T_{amb} = 0°C$			20			100	nA
V_i	Input voltage range		± 10			± 10			V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	90		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	74	92		74	92		dB
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ $V_o = \pm 10V$	94			94			dB
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 10			± 10			V
I_s	Supply current				35			200	μA
P_S	Power consumption				1.05			6	mW

ELECTRICAL CHARACTERISTICS for LS 776C
($V_s = \pm 3V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	$I_{SET} = 1.5\ \mu A$			$I_{SET} = 15\ \mu A$			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$		2	6		2	6	mV
I_{OS}	Input offset current			0.7	6		2	25	nA
I_b	Input bias current			2	10		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ $V_o = \pm 1V$	88	106					dB
		$R_L \geq 5\ k\Omega$ $V_o = \pm 1V$				88	106		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			5		mA
I_s	Supply current			13	20		130	170	μA
P_S	Power consumption			78	120		780	1020	μW
	Transient response (unity gain)	$V_i = 20\ mV$ $R_L \geq 5\ k\Omega$ $C_L \leq 100\ pF$							
	Rise time t_r			3			0.6		μs
	Overshoot ΔV_o			0			5		%
SR	Slew rate	$R_L \geq 5\ k\Omega$		0.03			0.35		V/μs
The following specifications apply for $T_{amb} = 0$ to 70°C									
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$			7.5			7.5	mV
I_{OS}	Input offset current	$T_{amb} = 70°C$			6			25	nA
		$T_{amb} = 0°C$			10			40	nA
I_b	Input bias current	$T_{amb} = 70°C$			10			50	nA
		$T_{amb} = 0°C$			20			100	nA
V_i	Input voltage range		± 1			± 1			V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	86		70	86		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	74	92		74	92		dB
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ $V_o = \pm 1V$	88						dB
		$R_L \geq 5\ k\Omega$ $V_o = \pm 1V$				88			dB
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 2	± 2.4					V
		$R_L \geq 5\ k\Omega$				± 2	± 2.1		V
I_s	Supply current				25			180	μA
P_S	Power consumption				150			1080	μW

Fig. 1 - Input bias current vs. set current

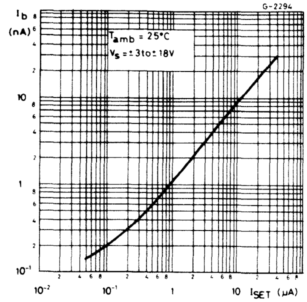


Fig. 2 - Input bias current vs. ambient temperature

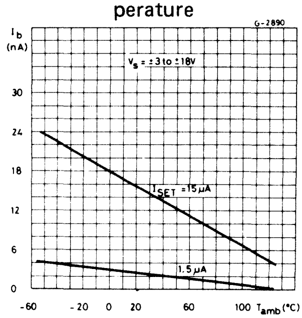


Fig. 3 - Input offset current vs. ambient temperature

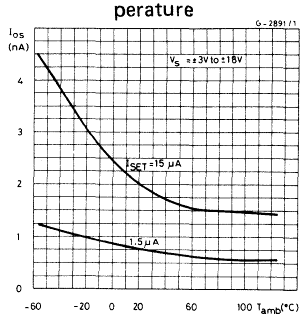


Fig. 4 - Change in input offset voltage vs. set current

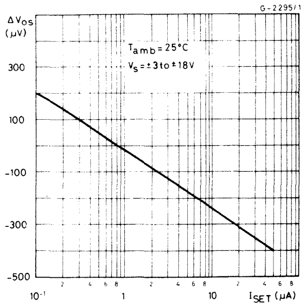


Fig. 5 - Change in input offset voltage vs. ambient temperature (unnulled)

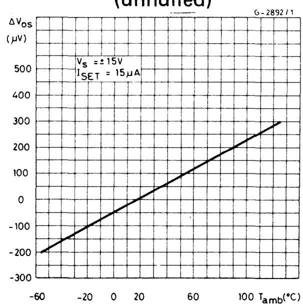


Fig. 6 - Input noise voltage vs. set current

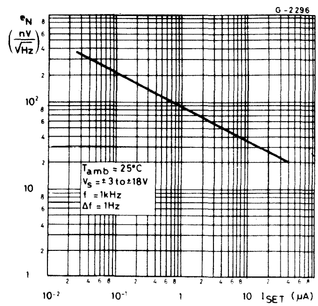


Fig. 7 - Input noise voltage and current vs. frequency

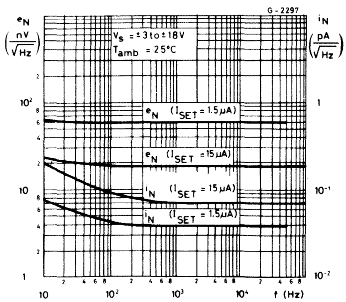


Fig. 8 - Input noise current vs. set current

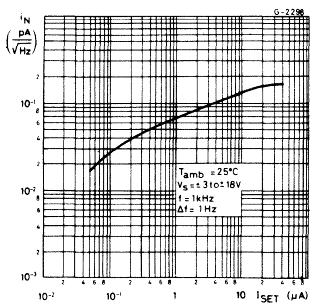


Fig. 9 - Optimum source resistance for minimum noise vs. set current.

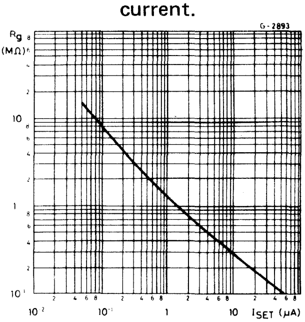


Fig. 10 - Output voltage swing vs. load resistance

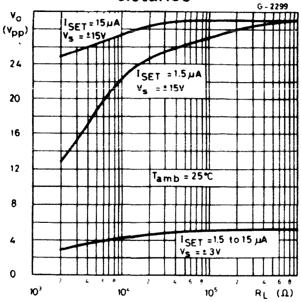


Fig. 11 - Output voltage swing vs. supply voltage

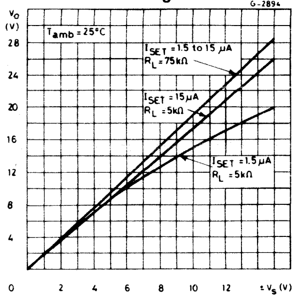


Fig. 12 - Gain bandwidth product vs. set current

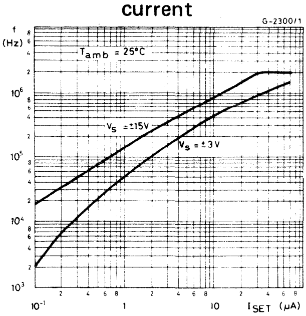


Fig. 13 - Open loop voltage gain vs. ambient temperature

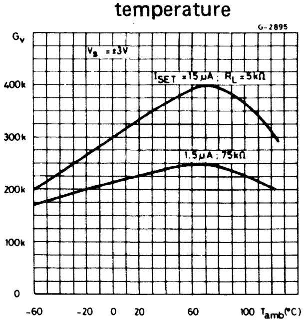


Fig. 14 - Open loop voltage gain vs. ambient temperature

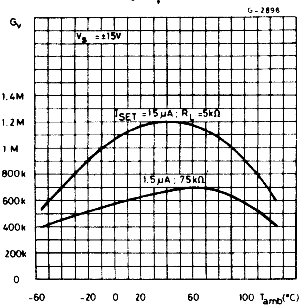


Fig. 15 - Open loop voltage gain vs. set current

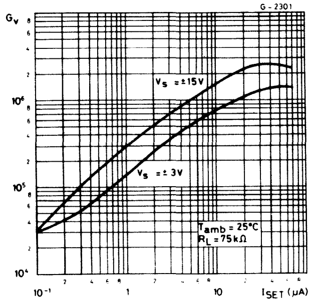


Fig. 16 - Common mode rejection vs. set current

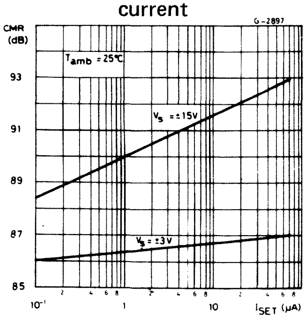


Fig. 17 - Supply voltage rejection vs. set current

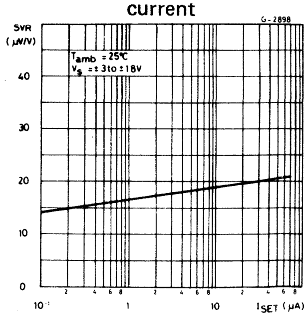


Fig. 18 - Supply current vs. ambient temperature

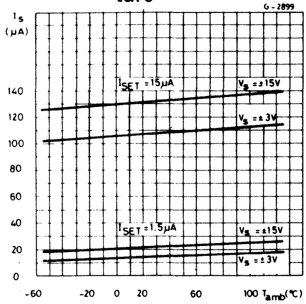


Fig. 19 - Standby supply current vs. set current

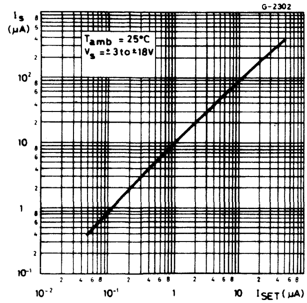


Fig. 20 - Slew rate vs. set current

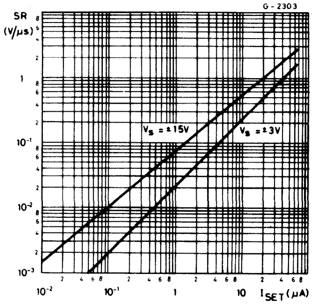
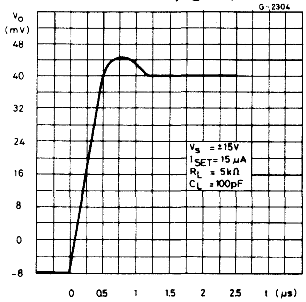


Fig. 21 - Voltage follower transient response (unity gain)



TYPICAL APPLICATIONS

Fig. 22 - High accuracy sample and hold

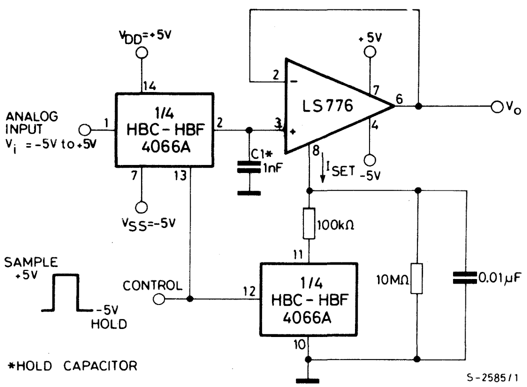


Fig. 23 - Nanowatt amplifier

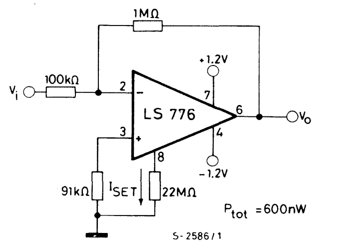
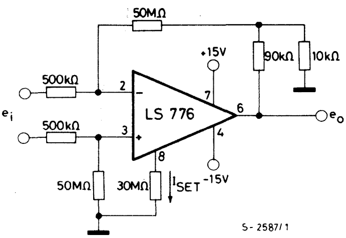


Fig. 24 - High input impedance amplifier



TYPICAL APPLICATIONS (continued)

Fig. 25 - Multiplexing and signal conditioning

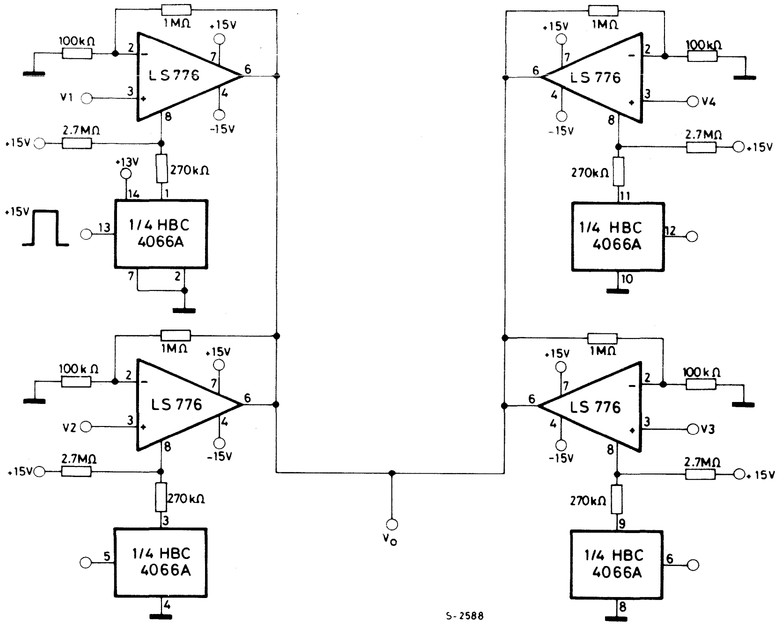


Fig. 26 - Multiple feedback bandpass filter

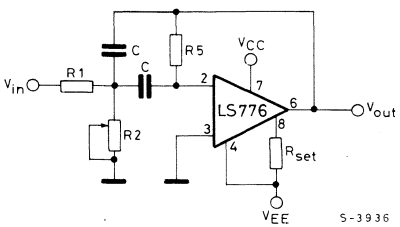
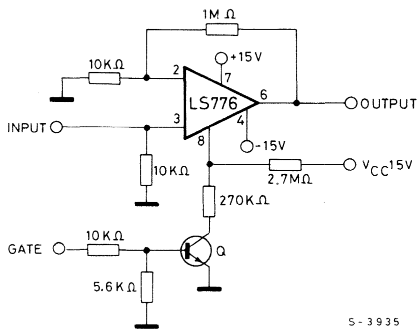


Fig. 27 - Gated amplifier



SGS LS 4558N

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH UNITY GAIN BANDWIDTH
- NO CROSSOVER DISTORTION
- NO POP NOISE
- SHORT CIRCUIT PROTECTION
- HIGH CHANNEL SEPARATION

The LS 4558N is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range and the specially designed input stage allow the LS 4558N to be used in **low noise audio signal processing application.** The optimized class AB output stage completely eliminates crossover distortion, under any load conditions, has large source and sink capacity and is short circuit protected.

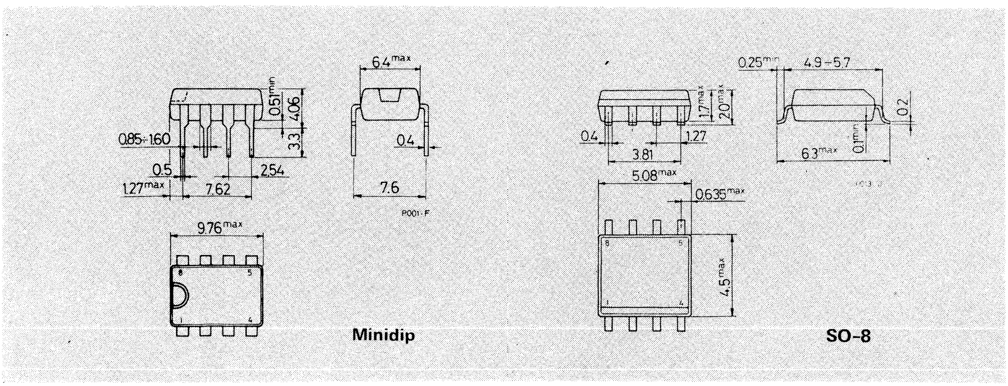
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_I	Input voltage		$\pm V_s$	
V_i	Differential input voltage		$\pm (V_s - 1)$	V
P_{tot}	Power dissipation at $T_{amb} = 70°C$	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

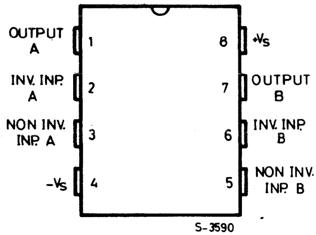
ORDERING NUMBER: LS 4558 NB (Minidip)
LS 4558 NM (Micropackage)

MECHANICAL DATA

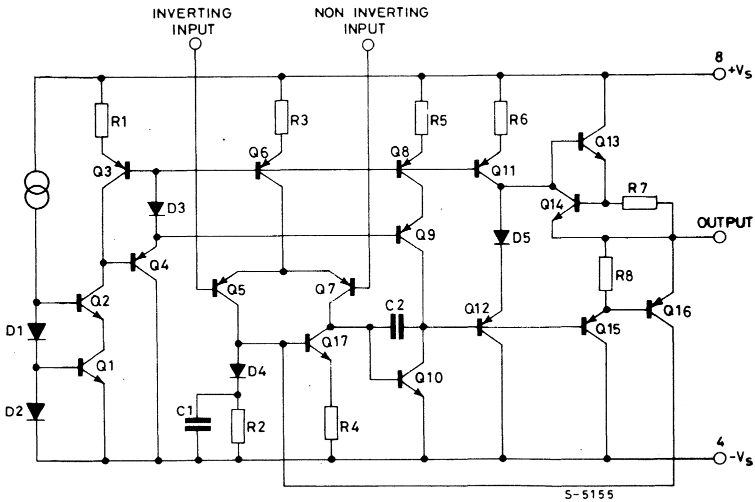
Dimensions in mm



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one section)



THERMAL DATA

		Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	120 °C/W	200* °C/W

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current (*)			1	2	mA
I_b	Input bias current			50	500	nA
		$T_{min} < T_{op} < T_{max}$			800	nA
R_i	Input resistance	f = 1 KHz	0.3	1		MΩ
V_{os}	Input offset voltage	$R_g \leq 10$ KΩ		0.5	5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			7.5	mV
I_{os}	Input offset current			20	200	nA
		$T_{min} < T_{op} < T_{max}$			500	nA
I_{sc}	Output short circuit current			23		mA
G_v	Large signal open loop voltage gain	R_L = 2 KΩ	86	100		dB
B	Gain-bandwidth product	f = 20 KHz	2	3		MHz
e_N	Total input noise voltage	f = 1 KHz R_g = 50Ω R_g = 1 KΩ R_g = 10 KΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
e_N	Popcorn noise	B = 1 Hz to 1 KHz R_g = 10 KΩ t = 10 sec			10	μV peak
d	Distortion	G_v = 20 dB R_L = 2 KΩ V_o = 2 Vpp f = 1 KHz		0.03		%
V_o	Output voltage swing	R_L = 2 KΩ		± 13		V
V_o	Large signal voltage swing	R_L = 10 KΩ f = 10 KHz		28		Vpp
Transient response	Rise time	V_i = 20 mV R_L = 2 KΩ C_L = 100 pF		0.13		μS
	Overshoot			5		%
SR	Slew rate	unity gain R_L = 2 KΩ	0.8	1.5		V/μs
CMR	Common mode rejection	V_i = 10V $T_{min} < T_{op} < T_{max}$	70	90		dB
SVR	Supply voltage rejection	V_i = 1V f = 100 Hz $T_{min} < T_{op} < T_{max}$	80	100		dB
CS	Channel separation	f = 10 KHz R_g = 1 KΩ		105		dB

(*) Both amplifiers.

Fig. 1 - Open loop frequency and phase response

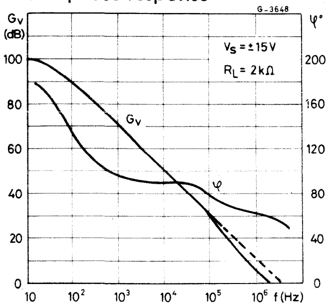


Fig. 2 - Open loop gain vs. ambient temperature

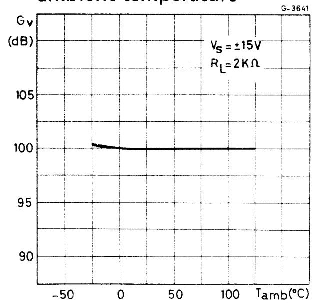


Fig. 3 - Supply voltage rejection vs. frequency

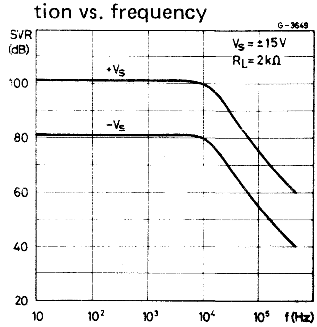


Fig. 4 - Large signal frequency response

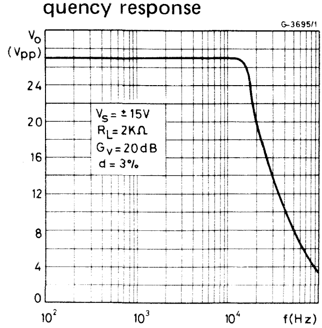


Fig. 5 - Output voltage swing vs. load resistance

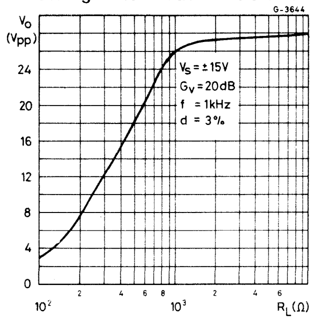


Fig. 6 - Total input noise vs. frequency

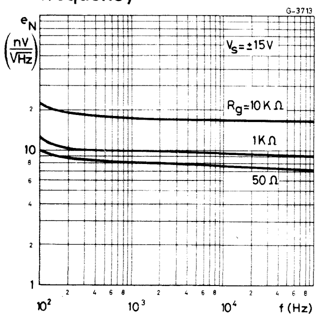


Fig. 7 - Channel separation

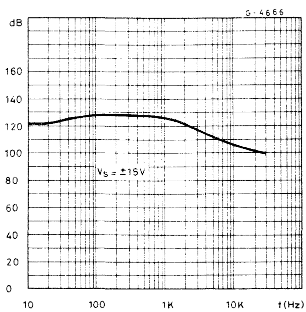


Fig. 8 - Transient response

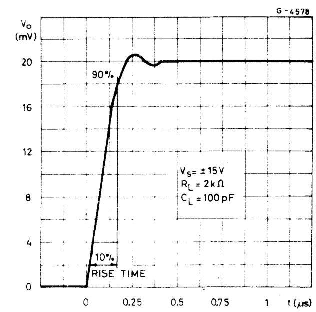
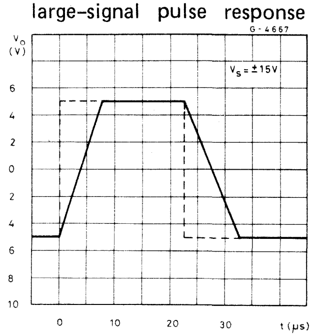
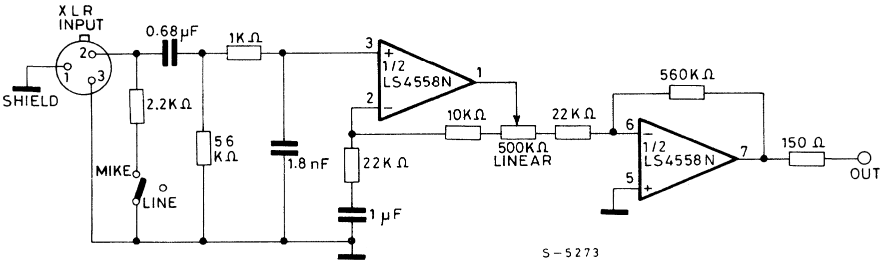


Fig. 9 - Voltage follower large-signal pulse response



APPLICATION INFORMATION

Fig. 10 - Mike/Line preamplifier for audio mixers (0 dB to 60 dB continuously variable gain)



Note — The particular characteristics of the circuit of fig. 10 is that using a linear potentiometer, the gain is continuously variable in a logarithmic mode from 0 dB to 60 dB in the audio band.

Fig. 11 - Microphones nomograph

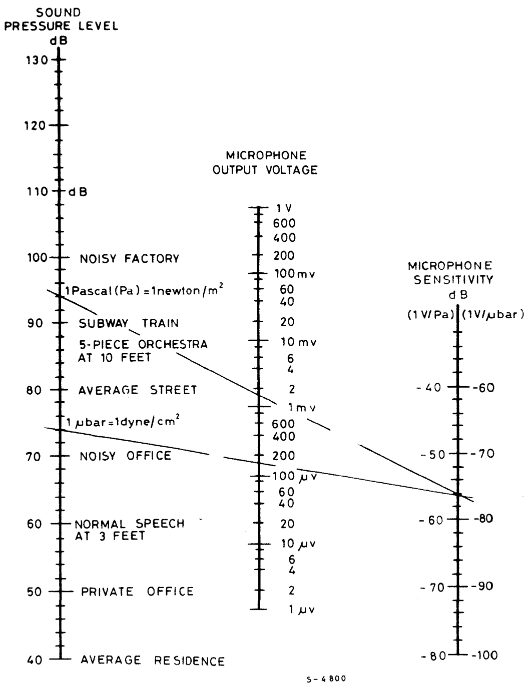


Fig. 12 - Very Low-Noise mike preamplifier (G_v= 40 dB)

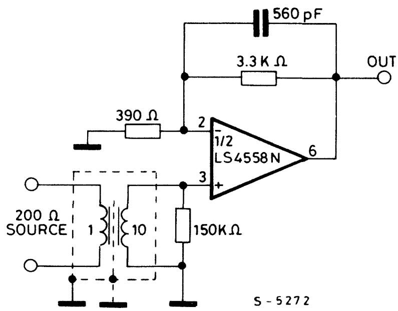
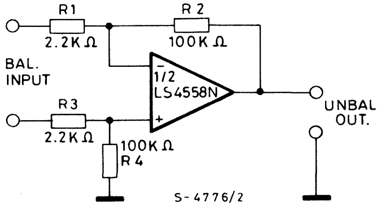


Fig. 13 - Balanced input audio preamplifier



APPLICATION INFORMATION (continued)

Fig. 14 - 20 Hz to 200 Hz variable High-pass filter (G_v = 3 dB)

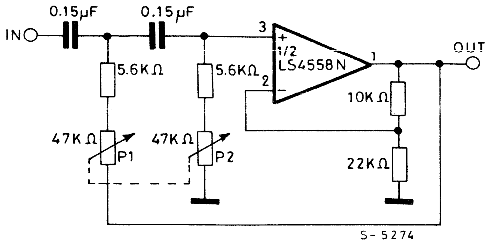


Fig. 15 - Frequency response of the High-pass filter of fig. 14

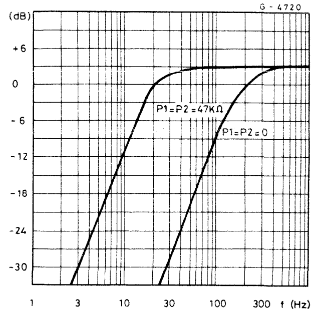


Fig. 16 - DC coupled low-pass active filter (f = 1KHz, G_v= 6 dB)

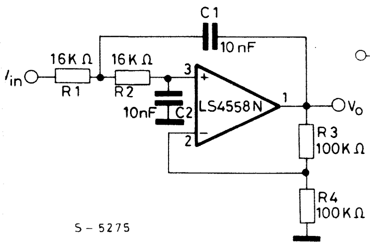


Fig. 17 - Switchable HP-LP audio filter

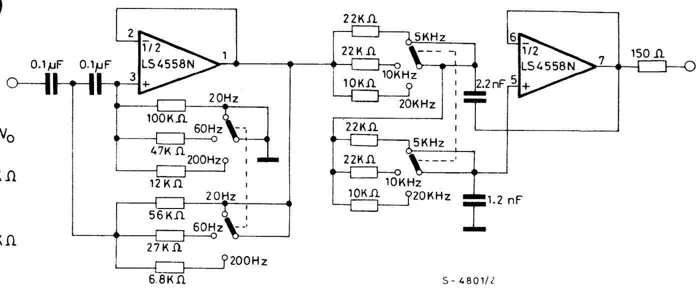
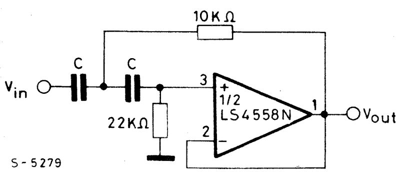
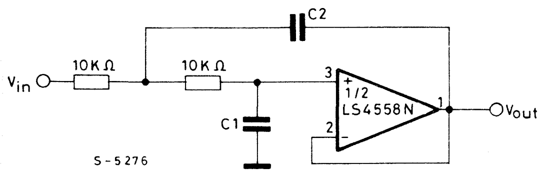


Fig. 18 - Subsonic or rumble filter (G_v= 0 dB)



f_c (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

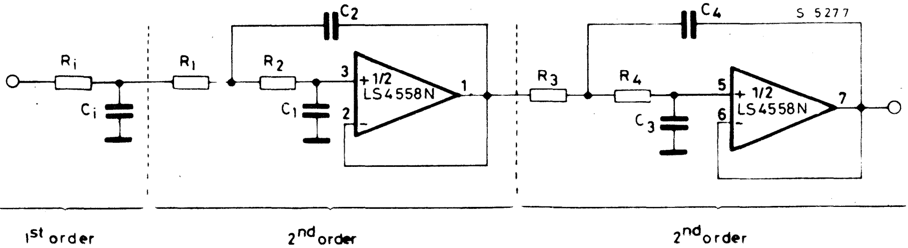
Fig. 19 - High-cut filter (G_v= 0 dB)



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 20 - Fifth order 3.4 KHz low-pass Butterworth filter



For $f_c = 3.4$ KHz and $R_i = R1 = R2 = R3 = R4 = 10\ K\Omega$, we obtain:

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

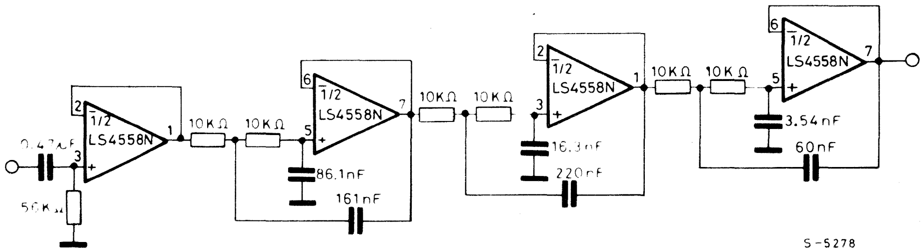
$$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 21 - Six-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

LINEAR INTEGRATED CIRCUITS

MC1458
MC1458C

PRELIMINARY DATA

DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY COMPENSATED
- SHORT-CIRCUIT PROTECTED
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

The MC 1458 is a dual operational amplifier with frequency and phase compensation built into the chip, available in 8-lead minidip package and in 8-lead micropackage. It is intended for a wide range of applications where space and cost saving are the main goals. In spite of that, the MC 1458 offers good performance and absence of latch-up makes the device ideal for use as voltage follower, integrator, summing amplifier and general feedback applications.

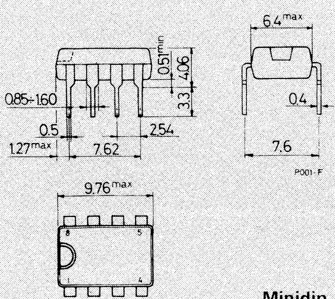
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_i	Input voltage (*)		± 15	V
V_i	Differential input voltage		± 30	V
P_{tot}	Power dissipation at T_{amb} = 70°C	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_{stg}	Storage temperature		-55 to 150	°C

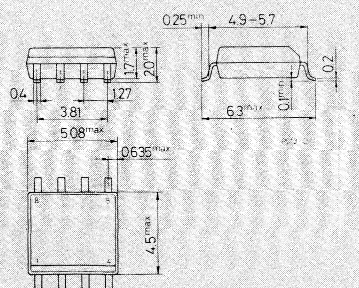
(*) For V_s lower than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

MECHANICAL DATA

Dimensions in mm



Minidip

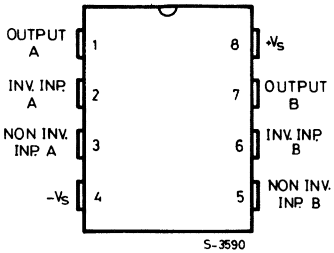


SO-8

8/83

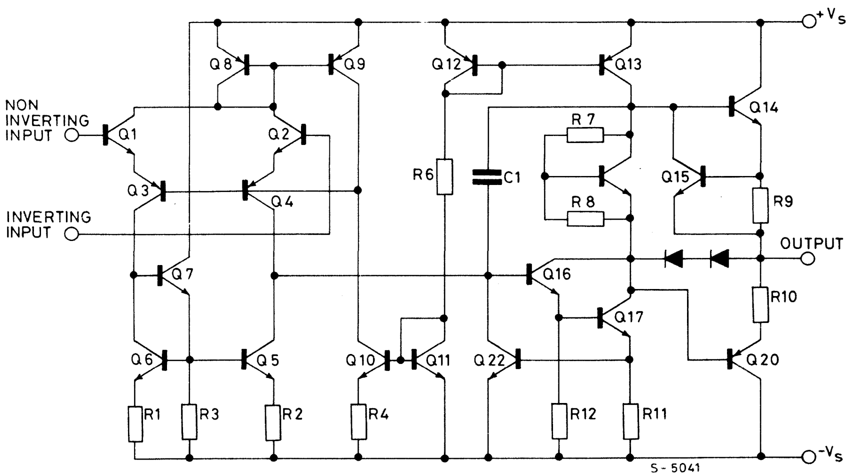
MC1458
MC1458C

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	Minidip	SO-8
MC 1458	MC 1458 P1	MC 1458 M
MC 1458C	MC 1458 CP1	MC 1458 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm.).

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	MC 1458			MC 1458C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current (both amplifiers)				5.6			8	mA
I_b	Input bias current				0.5			0.7	μA
		$0°C < T_{op} < 70°C$			0.8			1	μA
V_{os}	Input offset voltage	$R_g \leq 10\ K\Omega$		2	6		2	10	mV
		$R_g \leq 10\ K\Omega$, $0°C < T_{op} < 70°C$			7.5			12	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	$R_g = 10\ K\Omega$, $0°C < T_{op} < 70°C$		6			6		μV/°C
I_{os}	Input offset current			20	200		20	300	nA
		$0°C < T_{op} < 70°C$			300			400	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$0°C < T_{op} < 70°C$		0.5			0.5		nA/°C
I_{sc}	Output short circuit current			20			20		mA
G_v	Large signal open loop voltage gain	$R_L = 2K\Omega$, $T_{amb} = 0$ to $70°C$	83						dB
		$R_L = 2K\Omega$	86	106					dB
		$R_L = 10K\Omega$, $T_{amb} = 0$ to $70°C$				83			dB
		$R_L = 10K\Omega$				86	106		dB
B	Unity gain bandwidth			0.8			0.8		MHz
e_N	Input noise voltage	B= 10Hz to 10 KHz, $R_g = 1\ K\Omega$		3			3		μV
		B= 10Hz to 10 KHz, $R_g = 500\ K\Omega$		25			25		μV
V_o	Output voltage swing	$R_L = 2\ K\Omega$	± 10	± 13		± 9	± 13		V
		$R_L = 10\ K\Omega$	± 12	± 14		± 11	± 14		V
SR	Slew Rate		0.3			0.3			V/μs
CMR	Common mode rejection		70	90		60	90		dB
SVR	Supply voltage rejection		76	90			90		dB
	Common mode input voltage range		± 12	± 13		± 11	± 13		V

PRELIMINARY DATA

QUAD SINGLE-SUPPLY COMPARATOR

- WIDE OPERATING TEMPERATURE RANGE: -40 to +85°C
- SINGLE -SUPPLY OPERATION: +2.0 to +28 V
- DIFFERENTIAL INPUT VOLTAGE = ± V_s
- COMPARE VOLTAGES AT GROUND POTENTIAL
- TTL COMPATIBLE
- LOW CURRENT DRAIN
- OUTPUTS CAN BE CONNECTED TO GIVE THE IMPLIED AND FUNCTION

The MC3302 Quad Comparator is designed specifically for single positive supply consumer, automotive and industrial electronic applications. Each device contains four independent comparators, making it ideally suited to applications where high density and low cost are important.

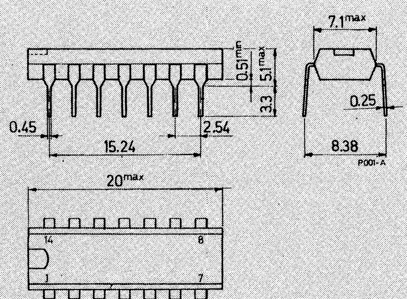
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	+2 to +28	V
V_I	Input voltage range	-0.3 to V_s	V
V_i	Differential input voltage	± V_s	
I_i	Input current (V_i < -0.3 V)	50	mA
P_{tot}	Total power dissipation at T_{amb} = 25°C	600	mW
T_{op}	Operating temperature	-40 to +85	°C
T_{stg}	Storage and junction temperature	-65 to 150	°C

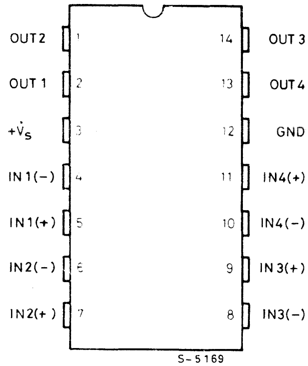
ORDERING NUMBER: MC 3302P

MECHANICAL DATA

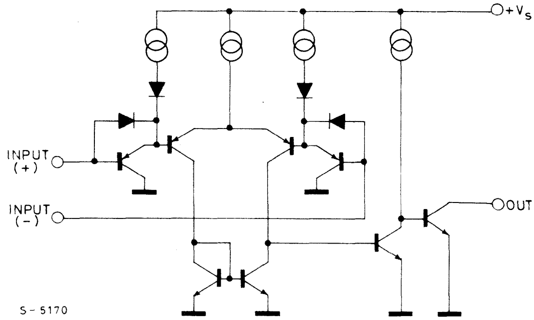
Dimensions in mm



CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



SCHEMATIC DIAGRAM
(each section)



THERMAL DATA

$R_{th\ j\text{–}amb}$	Thermal resistance junction-ambient	max 200 °C/W

ELECTRICAL CHARACTERISTICS (V_s = +15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{os}	Input offset voltage	V_{REF} = 1.2 V			3	20	mV
			T_{amb} = -40 to +85°C			40	
I_b	Input bias current (1)	Output in linear range			30	500	nA
			T_{amb} = -40 to +85°C			1000	
V_{ICR}	Input Common-Mode voltage range (2)	V_s = 28V		0 to 26			V
I_s	Supply current	$R_L = \infty$	V_s = 5V		0.8	1.8	mA
G_v	Voltage gain	R_L = 15 KΩ		66	90		dB
g_m	Transconductance				2		mhos
I_o	Output sink current	(V_s = 5.0 V) (T_{amb} = +25°C, V_{OL} = 400 mV)			6		mA
		(T_{amb} = -40 to +85°C, V_{OL} = 800 mV)		2			
V_{sat}	Output saturation voltage	$V_{IN(-)} \geq 1V$ $V_{IN(+)}$ = 0V I_{sink} = 2 mA	V_s = 5 to 28V		150	400	mV
$I_{o\ leak}$	Output leakage current	$V_{IN(+)} \geq 1V$ $V_{IN(-)}$ = 0V				1	μA
V_{IDR}	Differential input Voltage			±Vs			
CMR	Common Mode Rejection				60		dB
$t_{PHL/LH}$	Propagation delay time for positive and negative-going input pulse	R_L = 15KΩ			2		μs
t_{THL}	Transition Time	R_L = 15KΩ			0.15		μs
t_{TLH}					0.8		

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50 mA.

(3) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Fig. 1 - Supply current vs. voltage

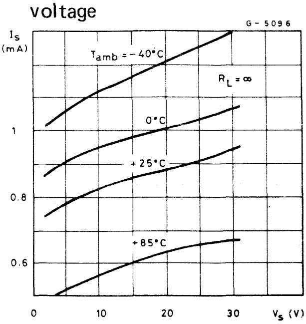


Fig. 2 - Input bias current vs. supply voltage

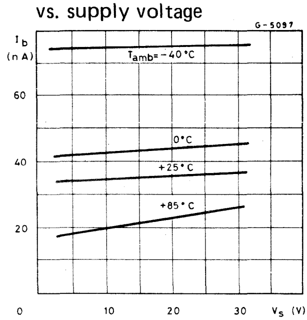


Fig. 3 - Normalized offset voltage vs. temperature

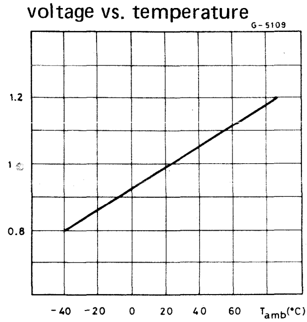


Fig. 4 - Output saturation voltage

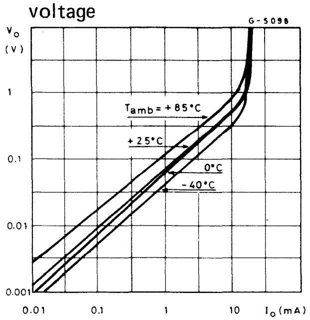


Fig. 5 - Response time

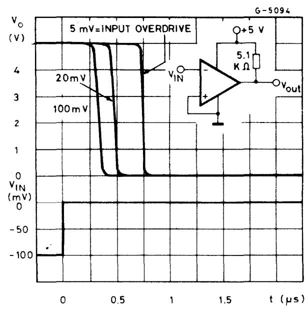
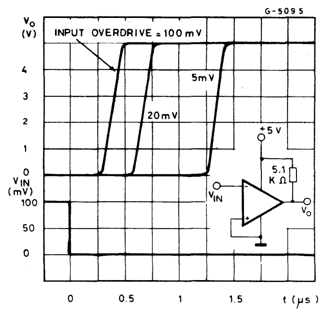


Fig. 6 - Reponse time



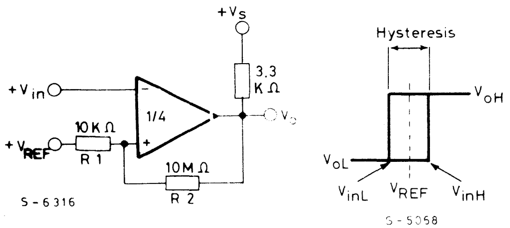
APPLICATION INFORMATION

The MC 3302 includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.
To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possibile.
It is good design practice to ground all unused pins.
The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

The output of the MC 3302 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.
The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximateely 60Ω r_{sat} of the output transistor.

APPLICATION INFORMATION (continued)

Fig. 7 - Comparator with Hysteresis



$$V_{in\,L} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Fig. 8 - Squarewave oscillator

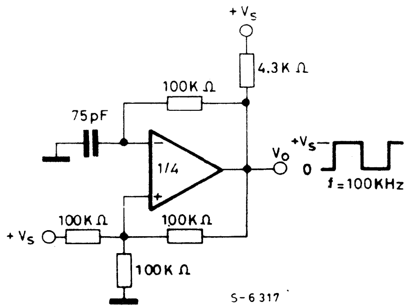


Fig. 9 - Time delay generator

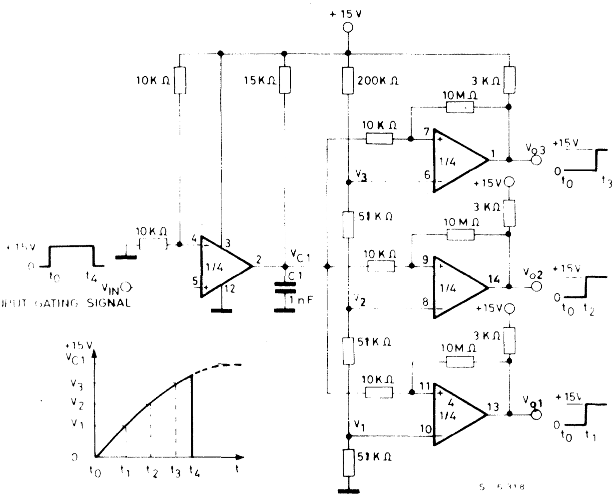
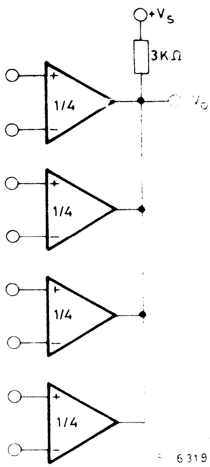


Fig. 10 - ORing the outputs



LINEAR INTEGRATED CIRCUITS

SGS **NE555**

TIMER

- TURN OFF TIME LESS THAN 2 μs
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

The NE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

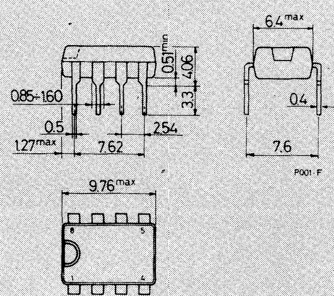
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Power dissipation at $T_{amb} \leq 60°C$	600	mW
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C

ORDERING NUMBER: NE555B

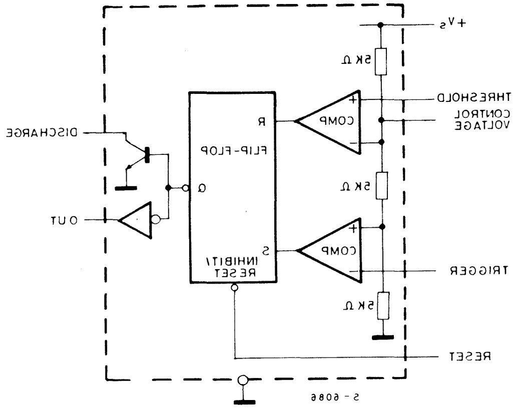
MECHANICAL DATA

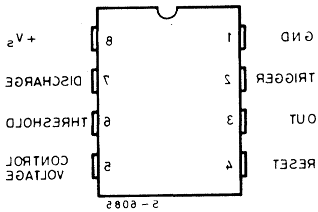
Dimensions in mm



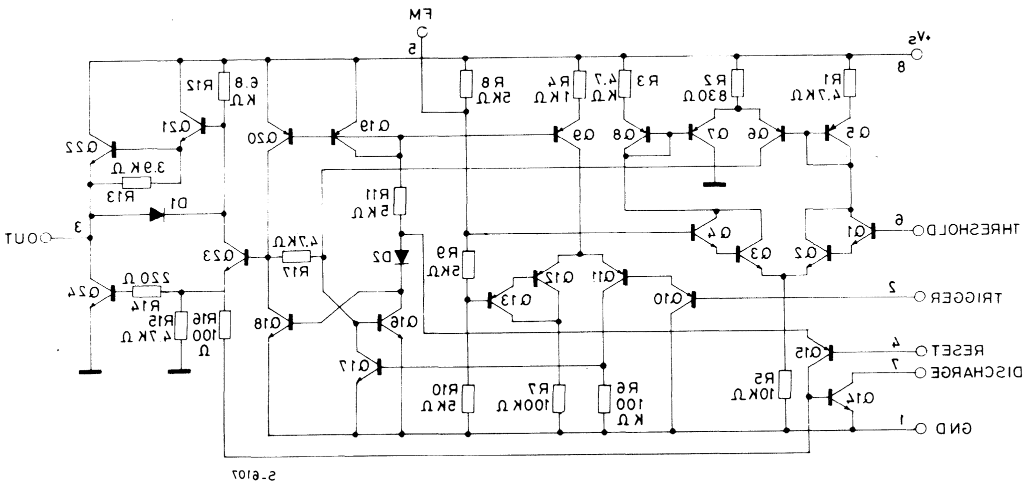
NE555

CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max 150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 5 to 15V unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4.5		16	V
I_s	Supply current (low state) (1)	V_s = 5V R_L = ∞ V_s = 15V R_L = ∞		3 10	6 15	mA mA
E_{tm}	Timing error (monostable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A = 2 to 100 KΩ C = 0.1 μF		 1 50 0.1	 3 0.5	 % ppm/°C %/V
E_{ta}	Timing error (astable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A, R_B = 1 to 100 KΩ C = 0.1 μF V_{cc} = 15V		 2.25 150 0.3		 % ppm/°C %/V
V_C	Control voltage level	V_s = 15V V_s = 5V	9 2.6	10 3.33	11 4	V V
V_T	Threshold voltage	V_s = 15V V_s = 5V	8.8 2.4	10 3.33	11.2 4.2	V V
I_T	Threshold current (3)			0.1	0.25	μA
V_{TR}	Trigger voltage	V_s = 15V V_s = 5V	4.5 1.1	5 1.67	5.6 2.2	V V
I_{TR}	Trigger current	V_{TR} = 0		0.5	2	μA
V_R	Reset voltage (4)		0.4	0.7	1	V
I_R	Reset current	V_R = 0		0.4 0.1	1.5 0.4	mA mA
V_{OL}	Output voltage (low)	V_s = 15V I_{SINK} = 10mA I_{SINK} = 50mA I_{SINK} = 100mA I_{SINK} = 200mA V_s = 5V I_{SINK} = 8mA I_{SINK} = 5mA		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	 V V V V V V

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output voltage (high)	V_s = 15V I_{SOURCE} = 200mA I_{SOURCE} = 100mA V_s = 5V I_{SOURCE} = 100mA	 12.75 2.75	 12.5 13.3 3.3		 V V V
t_{off}	Turn off time (5)	$V_{RESET} = V_s$		0.5		μs
t_r	Rise time of output			100	300	ns
t_f	Fall time of output			100	300	ns
I_L	Discharge leakage current			20	100	nA

NOTES

1. Supply current when output high typically 1mA less.
2. Tested at V_S = 5V and V_S = 15V
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total R = 10 MΩ, and for 5V operation, the max total R = 3.4 MΩ.
4. Specified with triggered input high.
5. Time measured from a positive going input pulse from 0 to 0.8 x V_s into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

Fig. 1 – Minimum pulse width required for triggering

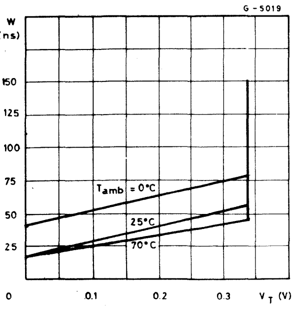


Fig. 2 - Total supply current vs. supply voltage

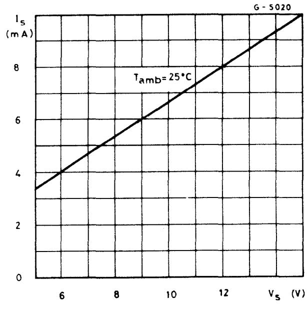


Fig. 3 - High output voltage vs. output source current

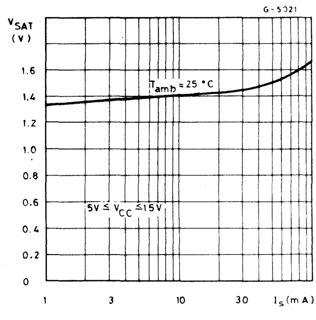


Fig. 4 - Low output voltage vs. output sink current

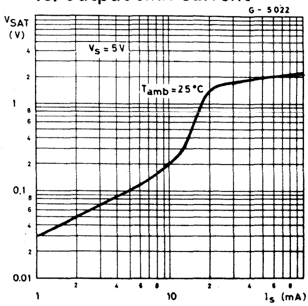


Fig. 5 - Low output voltage vs. output source current

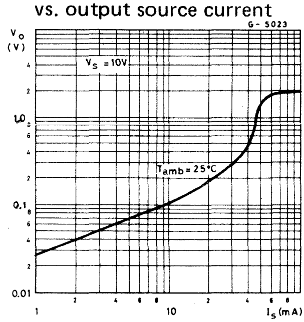


Fig. 6 - Low output voltage vs. output sink current

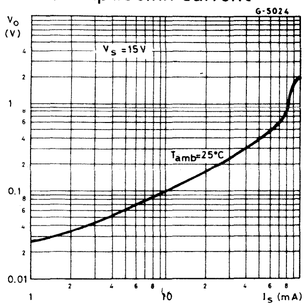


Fig. 7 - Normalized delay time vs. supply voltage

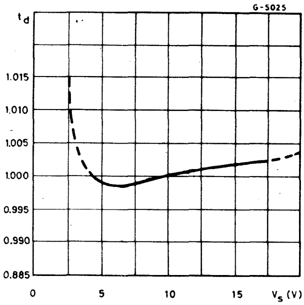


Fig. 8 - Normalized delay time vs. ambient temperature

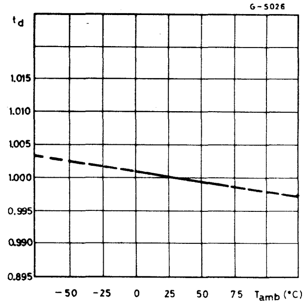
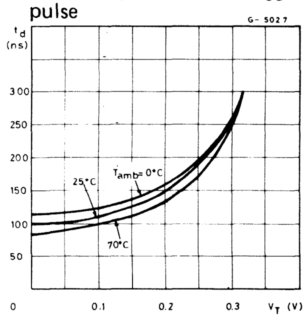


Fig. 9 - Propagation delay vs. voltage level of trigger pulse



APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_S. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R1C1$ and is easily determined by Figure 12. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

APPLICATION INFORMATION (Continued)

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals 2/3 V_s, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 11 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibly of false triggering.

Fig. 10

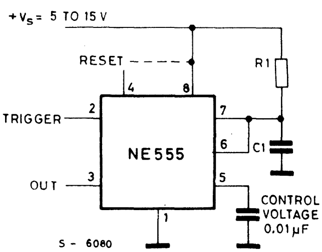


Fig. 11

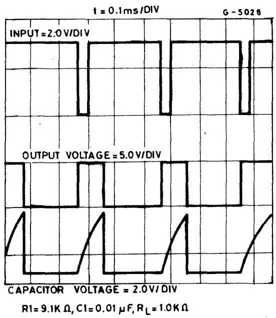
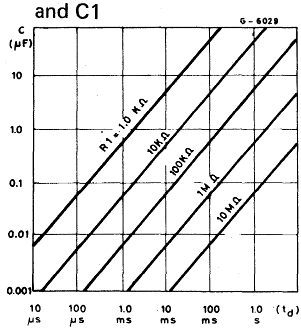


Fig. 12 - Time Delay vs R1 and C1



ASTABLE OPERATION

When the circuit is connected as shown in Figure 13 (pins 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_s and 2/3 V_s. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 14 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\,(R1 + R2)\,C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\,(R2)\,C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\,(R1 + 2R2)\,C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\,C1}$$

and may be easily found by Figure 15

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

Fig. 13

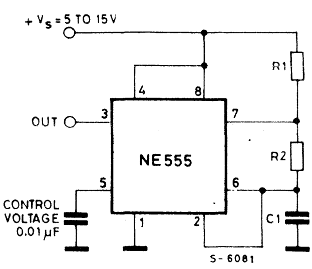


Fig. 14

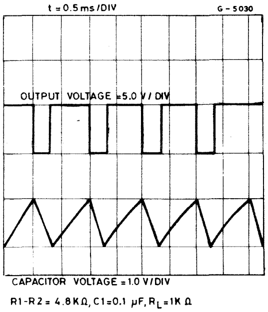
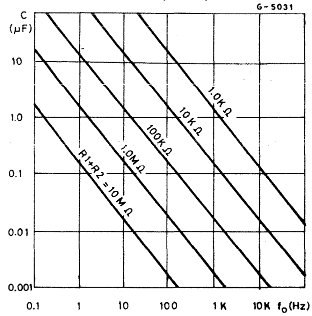


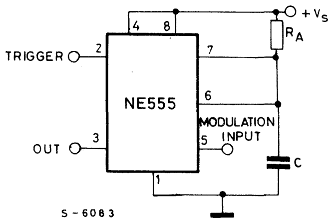
Fig. 15 - Free Running Frequency vs R1, R2, and C1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

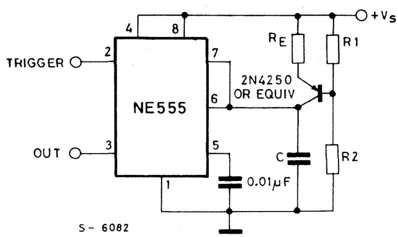
Fig. 16 - Pulse Width Modulator



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17



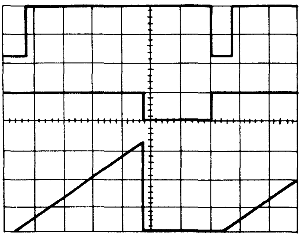
APPLICATION INFORMATION (Continued)

Figure 18 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\, V_s\, R_E\, (R_1 + R_2)\, C}{R_1\, V_s - V_{BE}\, (R_1 + R_2)} \qquad V_{BE} \simeq 0.6V$$

Fig. 18 - Linear ramp.



V_s = 5V
TIME = 20μs/DIV
R_1 = 47KΩ
R_2 = 100KΩ
R_E = 2.7KΩ
C = 0.01 μF

Top trace: input 3V/Div
Middle trace: output 5V/DIV
Bottom trace: output 5V/DIV
Bottom trace: capacitor voltage 1V/DIV

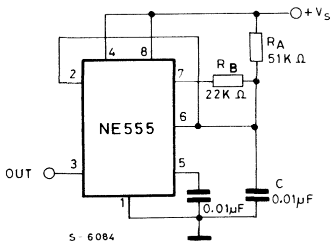
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in Figure 19. The time period for the output high is the same as previous, $t_1 = 0.693\, R_A\, C$. For the output low it is $t_2 =$

$$[(R_A\, R_B)/(R_A + R_B)]\, C Ln \left\{ \frac{R_B - 2R_A}{2R_B - R_A} \right\}$$

Thus the frequency of oscillation is $f = \dfrac{1}{t_1 + t_2}$

Figure 19 - 50% Duty cycle oscillator



Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_s and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

LINEAR INTEGRATED CIRCUITS

SGS NE556

DUAL TIMER

- TIMING FROM MICROSECONDS TO HOURS
- REPLACES TWO 555 TIMERS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

The NE 556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The NE 556 is a dual NE 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each sharing only V_S and ground. The circuits may be triggered and reset on falling waveforms. The output structures can sink or source up to 200 mA.

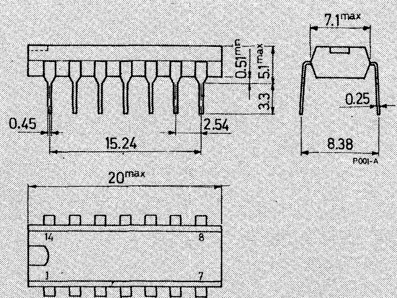
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Power dissipation at $T_{amb} \leq 60°C$	600	mW
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C

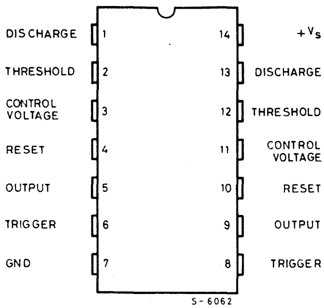
ORDERING NUMBER: NE556B

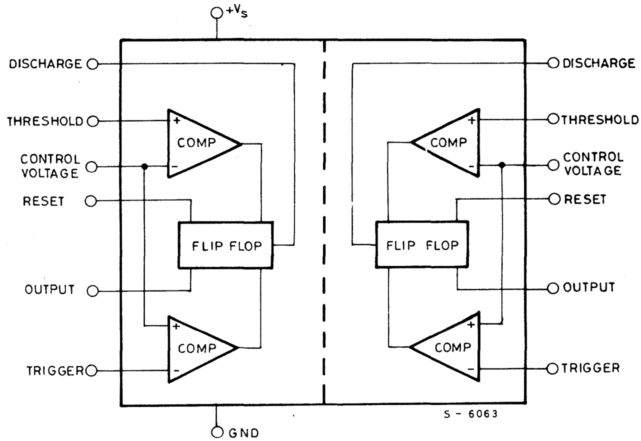
MECHANICAL DATA

Dimensions in mm

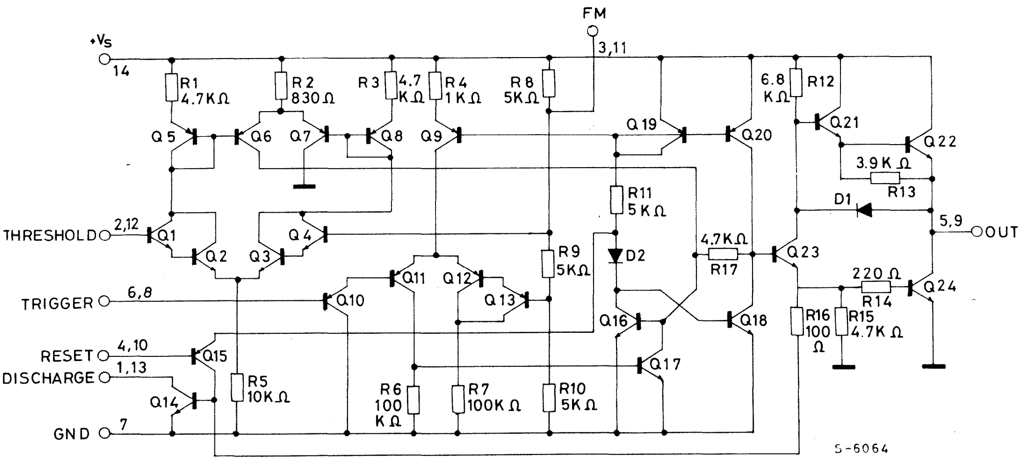


CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max. 150 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 5 to 15V unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4.5		16	V
I_s	Supply current (low state) (1)	V_s = 5V $R_L = \infty$ V_s = 15V $R_L = \infty$		6 20	12 30	mA mA
E_{tm}	Timing error (monostable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A = 2 to 100 KΩ C = 0.1 μF		 0.75 50 0.1	 3 0.5	 % ppm/°C %/V
E_{ta}	Timing error (astable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A, R_B = 1 to 100 KΩ C = 0.1 μF V_s = 15V		 2.25 150 0.3		 % ppm/°C %/V
V_C	Control voltage level	V_s = 15V V_s = 5V	9 2.6	10 3.33	11 4	V V
V_T	Threshold voltage	V_s = 15V V_s = 5V	8.8 2.4	10 3.33	11.2 4.2	V V
I_T	Threshold current (3)			30	250	nA
V_{TR}	Trigger voltage	V_s = 15V V_s = 5V	4.5 1.1	5 1.67	5.6 2.2	V V
I_{TR}	Trigger current	V_{TR} = O		0.5	2	μA
V_R	Reset voltage (5)		0.4	0.7	1	V
I_R	Reset current	 V_R = O		0.1 0.4	0.6 1.5	mA mA
V_{OL}	Output voltage (low)	V_s = 15V I_{SINK} = 10mA I_{SINK} = 50mA I_{SINK} = 100mA I_{SINK} = 200mA V_s = 5V I_{SINK} = 8mA I_{SINK} = 5mA		 0.1 0.4 2 2.5 0.25 0.15	 0.25 0.75 3.2 0.3 0.25	 V V V V V V

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output voltage (high)	V_s = 15V I_{SOURCE} = 200mA I_{SOURCE} = 100mA V_s = 5V I_{SOURCE} = 100mA	 12.75 2.75	 12.5 13.3 3.3		 V V V
t_r	Rise time of output			100	300	ns
t_f	Fall time of output			100	300	ns
I_L	Discharge leakage current			20	100	nA
C_M	Matching characteristics (4) Initial accuracy (2) Drift with temperature Drift with supply voltage			 1 10 0.2	 2 0.5	 % ppm/°C %/V

NOTES

1. Supply current when output high typically 1mA less.
2. Tested at V_s = 5V and V_s = 15V
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total R = 10 megohm, and for 5V operation, the max total R = 3.4 megohm.
4. Specified with triggered input high.
5. Time measured from a positive going input pulse from 0 to 0.8 x V_s into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

Fig. 1 - Minimum pulse width required for triggering

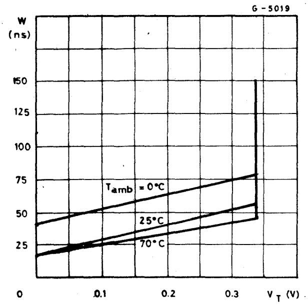


Fig. 2 - Total supply current vs. supply voltage

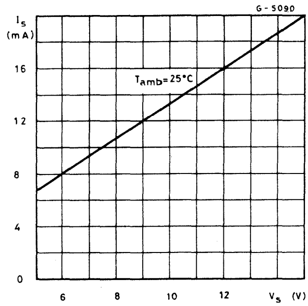


Fig. 3 - High output voltage vs output source current

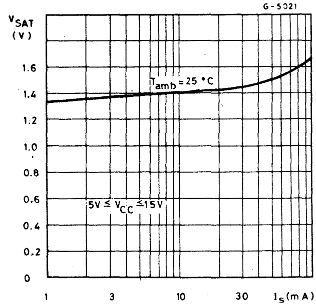


Fig. 4 - Low output voltage vs. output sink current

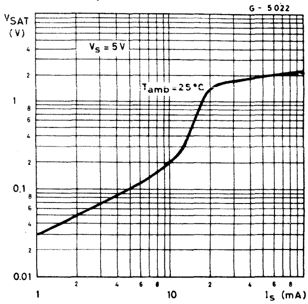


Fig. 5 - Low output voltage vs. output sink current

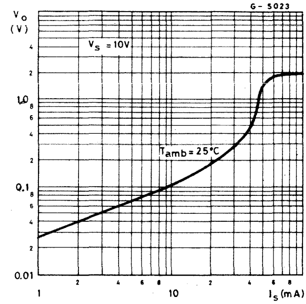


Fig. 6 - Low output voltage vs. output sink current

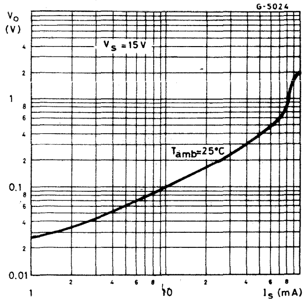


Fig. 7 - Normalized delay time vs. supply voltage

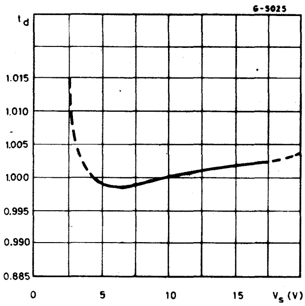


Fig. 8 - Normalized delay time vs. ambient temperature

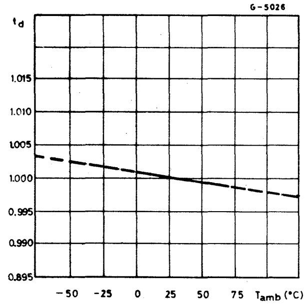
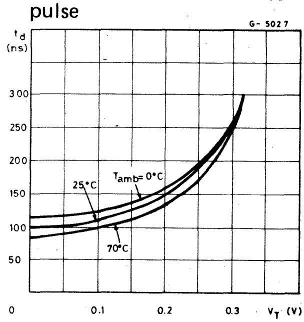


Fig. 9 - Propagation delay vs. voltage level of trigger pulse



APPLICATION INFORMATION

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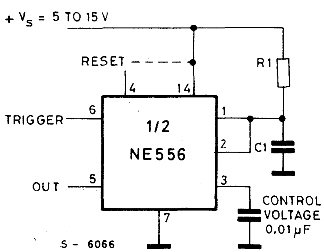
Fig. 10



TYPICAL APPLICATIONS (Continued)

When a negative trigger pulse is applied to pin 6, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals 2/3 V_s, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 11 shows the actual waveforms generated in this mode cooperation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_s. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by Figure 12. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 6) during the timing cycle discharge the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibly of false triggering.

Fig. 11

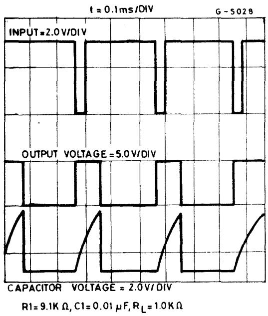
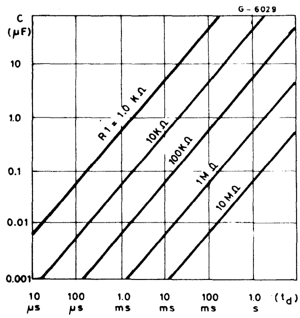


Fig. 12



ASTABLE OPERATION

When the circuit is connected as shown in Figure 13 (pins 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

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and the discharge time (output LOW) by:

$$t_2 = 0.693\,(R2)\,C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\,(R1 + 2R2)\,C1$$

The freqyency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 15.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

Fig. 13

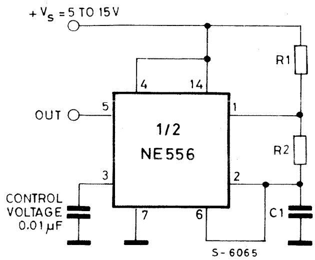


Fig. 14

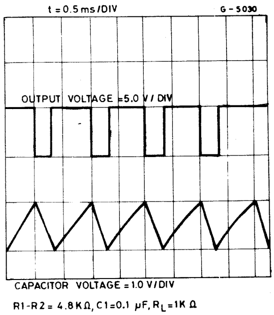
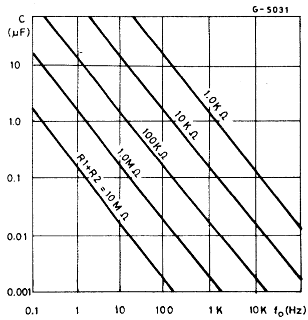


Fig. 15 - Free Running Frequency vs R1, R2 and C1



LINEAR INTEGRATED CIRCUITS

GENERAL PURPOSE TRANSISTOR ARRAY

The TBA 331 is an array of 5 monolithic NPN transistors in a 14-lead dual in-line plastic package. Two transistors are internally connected to form a differential amplifier.
The transistors of the TBA 331 are well suited to low noise general purpose and to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete components in conventional circuits; in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

ABSOLUTE MAXIMUM RATINGS

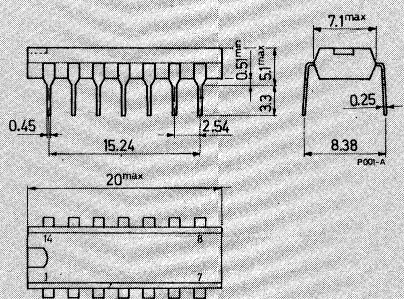
		Each transistor	Total package	
V_{CBO}	Collector-base voltage ($I_E = 0$)	20	–	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	15	–	V
V_{CSS}*	Collector-substrate voltage	20	–	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	5	–	V
I_C	Collector current	50	–	mA
P_{tot}	Total power dissipation at $T_{amb} \leq 55°C$	300	750	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150		°C
T_{op}	Operating temperature	0 to 85		°C

* The collector of each transistor of the TBA 331 is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

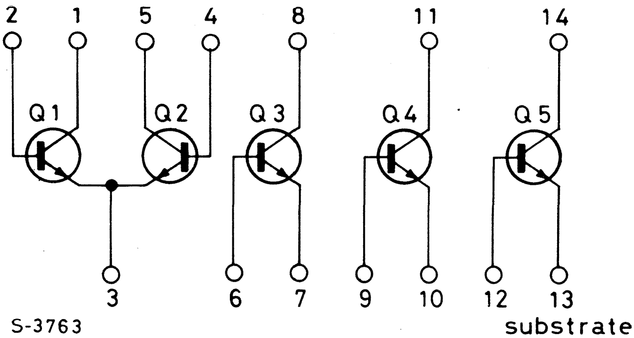
ORDERING NUMBER: TBA 331

MECHANICAL DATA

Dimensions in mm



SCHEMATIC DIAGRAM



THERMAL DATA

			each	Total
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	315° C/W	126° C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current ($I_E = 0$)	V_{CB} = 10 V		0.002	40	nA
I_{CEO}	Collector cutoff current ($I_B = 0$)	V_{CE} = 10 V		see curve	0.5	μA
$\lvert I_{B1} - I_{B2} \rvert$	Input offset current	I_C = 1 mA V_{CE} = 3 V		0.3	2	μA

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CBO}	Collector-base voltage ($I_E = 0$)	I_C = 10 µA	20	60		V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	I_C = 1 mA	15	24		V
V_{CSS}	collector-substrate voltage ($I_{CSS} = 0$)	I_C = 10 µA	20	60		V
$V_{CE\ (sat)}$	Collector-emitter saturation voltage	I_B = 1 mA I_C = 10 mA		0.23		V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	I_E = 10 µA	5	7		V
V_{BE}	Base-emitter voltage	I_E = 1 mA V_{CE} = 3 V		0.715		V
		I_E = 10 mA V_{CE} = 3 V		0.8		V
$\|V_{BE1}-V_{BE2}\|$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\|V_{BE3}-V_{BE4}\|$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\|V_{BE4}-V_{BE5}\|$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\|V_{BE5}-V_{BE4}\|$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Base-emitter voltage temperature coefficient	I_C = 1 mA V_{CE} = 3 V		-1.9		mV/°C
$\frac{\|V_{BE1}-V_{BE2}\|}{\Delta T}$	Input offset voltage temperature coefficient	I_C = 1 mA V_{CE} = 3 V		1.1		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
h_{FE}	DC current gain	I_C = 10 mA, V_{CE} = 3 V		100		–
		I_C = 1 mA, V_{CE} = 3 V	40	100		–
		I_C = 10 μA, V_{CE} = 3 V		54		–
f_T	Transition frequency	I_C = 3 mA, V_{CE} = 3 V	300	550		MHz
NF	Noise figure	I_C = 100 μA, V_{CE} = 3 V, f = 1 KHz, R_g = 1 kΩ		3.25		dB
H_{ie}	Input impedance	I_C = 1 mA, V_{CE} = 3 V, f = 1 kHz		3.5		kΩ
h_{fe}	Forward current transfer ratio	I_C = 1 mA, V_{CE} = 3 V, f = 1 kHz		110		–
h_{re}	Reverse voltage transfer ratio	I_C = 1 mA, V_{CE} = 3 V, f = 1 kHz		1.8×10^{-4}		–
h_{oe}	Output admittance	I_C = 1 mA, V_{CE} = 3V, f = 1 kHz		15.6		μS
y_{ie}	Input admittance	I_C = 1 mA, V_{CE} = 3 V, f = 1 MHz		0.3+j0.04		mS
y_{fe}	Forward transadmittance	I_C = 1 mA, V_{CE} = 3 V, f = 1 MHz		31–j1.5		mS
y_{re}	Reverse transadmittance	I_C = 1 mA, V_{CE} = 3 V, f = 1 MHz		see curve		mS

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
y_{ce}	Output admittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		0.001+j0.03		mS
C_{EBO}	Emitter-base capacitance	I_C = 0 V_{EB} = 3 V		0.6		pF
C_{CBo}	Collector-base capacitance	I_E = 0 V_{CB} = 3 V		0.58		pF
C_{CSS}	Collector-sustrate capacitance	I_C = 0 V_{CSS} = 3 V		2.8		pF

Fig. 1 - Collector cutoff current vs ambient temperature

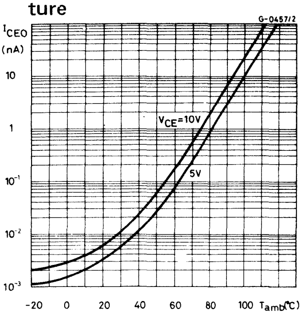


Fig. 2 - DC current gain vs. emitter current.

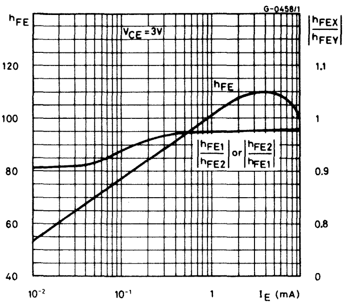


Fig. 3 - Input voltage and input offset voltage vs. emitter current

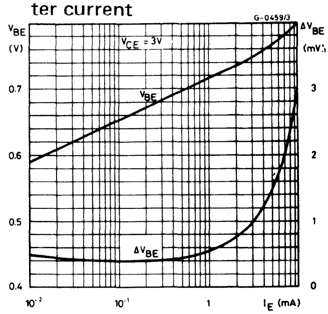


Fig. 4 - Input characteristic for each transistor

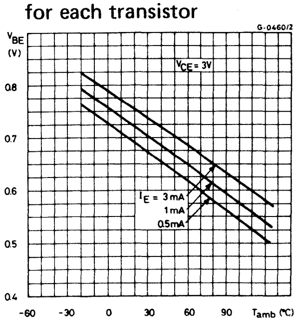


Fig. 5 - Input offset voltage vs. ambient temperature

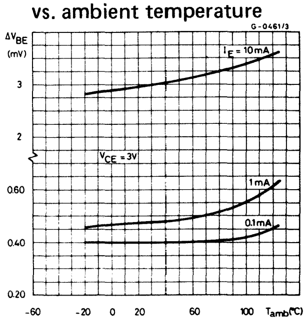


Fig. 6 - Input offset current for matched transistor pair

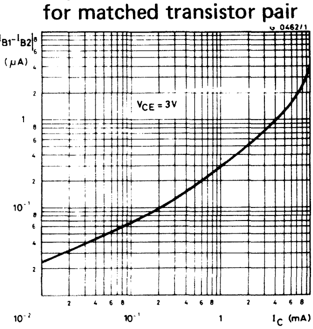


Fig. 7 - Noise figure vs collector current

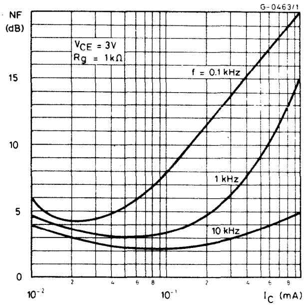


Fig. 8 - Forward admittance

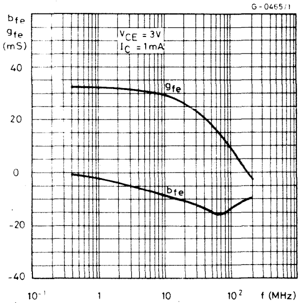


Fig. 9 - Input admittance

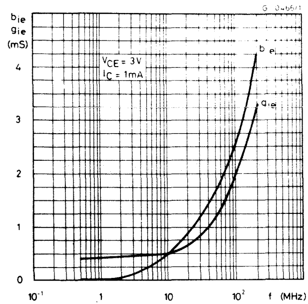


Fig. 10 - Output admittance

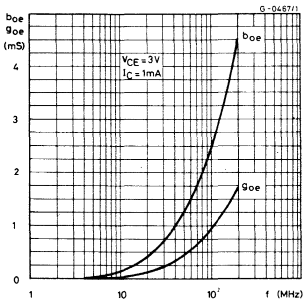


Fig. 11 - Reverse admittance

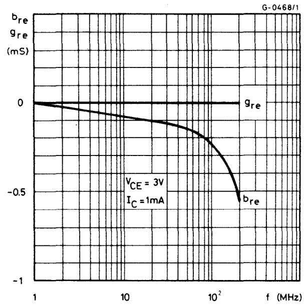
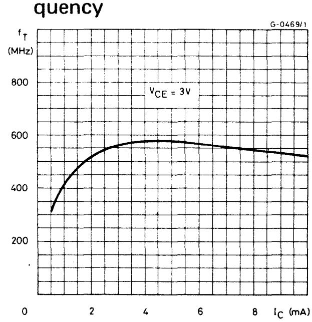


Fig. 12 - Transition frequency



SGS **TDA 2320**

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

The TDA 2320 is a monolithic integrated circuit in Minidip package specially designed to amplify the IR signal in remote controlled TV or radio sets. It directly interfaces with the digital control circuitry.
The TDA 2320 incorporates a two stages amplifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and flash or carrier transmission modes as provided for example by the M709/M710C/MOS transmitter.
The TDA 2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.

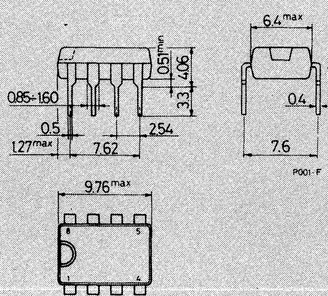
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
$T_{stg,\ j}$	Storage and Junction temperature	-40 to 150	°C
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW

ORDERING NUMBER: TDA 2320

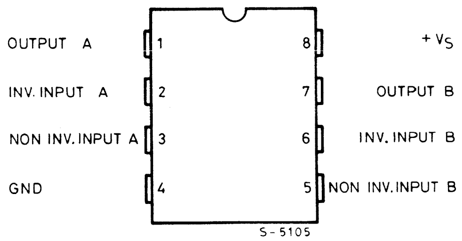
MECHANICAL DATA

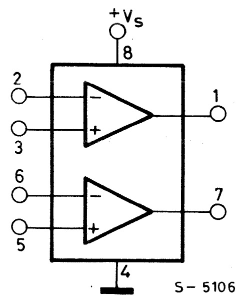
Dimensions in mm



CONNECTION AND BLOCK DIAGRAM

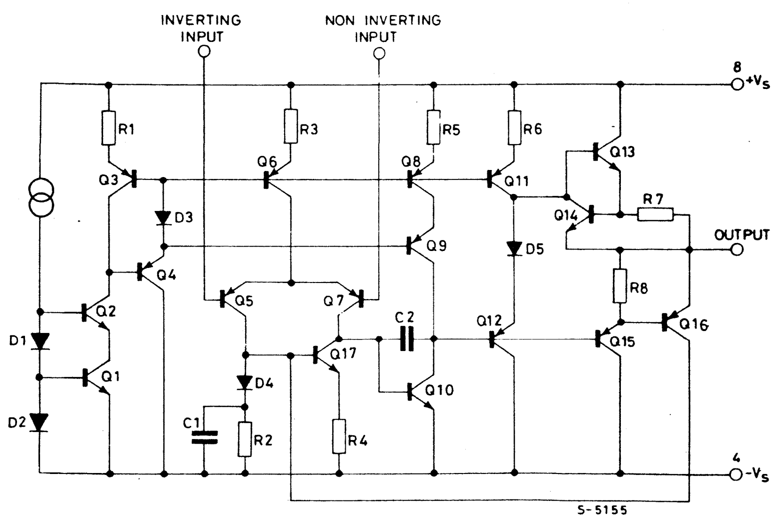
(top view)





SCHEMATIC DIAGRAM

(one section)



THERMAL DATA

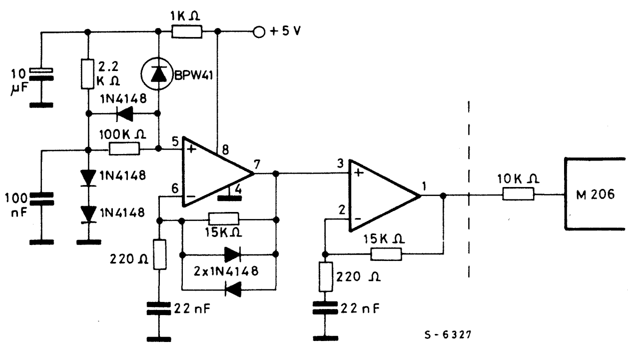
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 5V, T_{amb}= 25°C, single amplifier, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_s	Total supply current	V_s = 20V		0.8	2	mA
I_b	Input bias current			100	500	nA
V_{os}	Input offset voltage	R_g < 10 KΩ		0.5		mV
I_{os}	Input offset current			15		nA
G_v	Open loop voltage gain	f = 1 KHz	64	70		dB
		f = 100 KHz		30		dB
B	Gain bandwidth product	f = 40 KHz	1.5	3		MHz
SR	Slew rate	R_L= 2 KΩ		1.5		V/µs
e_N	Total input noise voltage	f = 40 KHz Rg= 10KΩ		20		$nV/\sqrt{Hz}$
V_o.	DC output voltage swing			2.5		Vpp
SVR	Supply voltage rejection	f = 100 Hz		80		dB

APPLICATION INFORMATION

Fig. 1 – Application circuit for carrier transmission mode



APPLICATION INFORMATION (continued)

Fig. 2 - Flash mode preamplifier

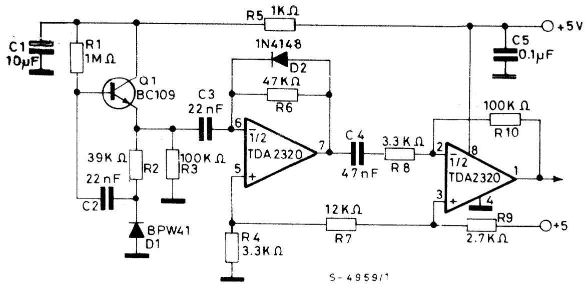


Fig. 3 - P.C. and components layout of the circuit of fig. 2 (1 : 1 scale)

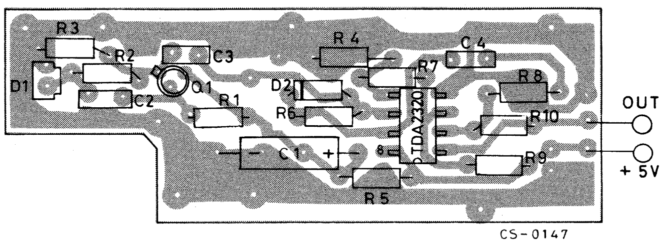


Fig. 4 - IR transmitter using M709 or M710

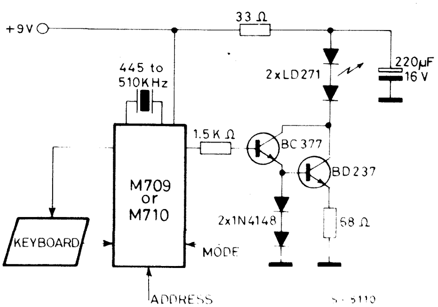
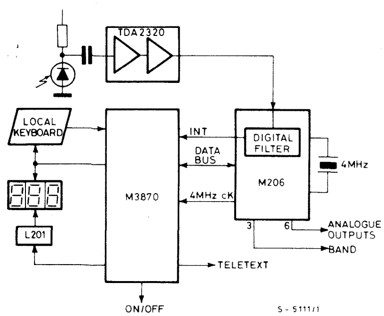
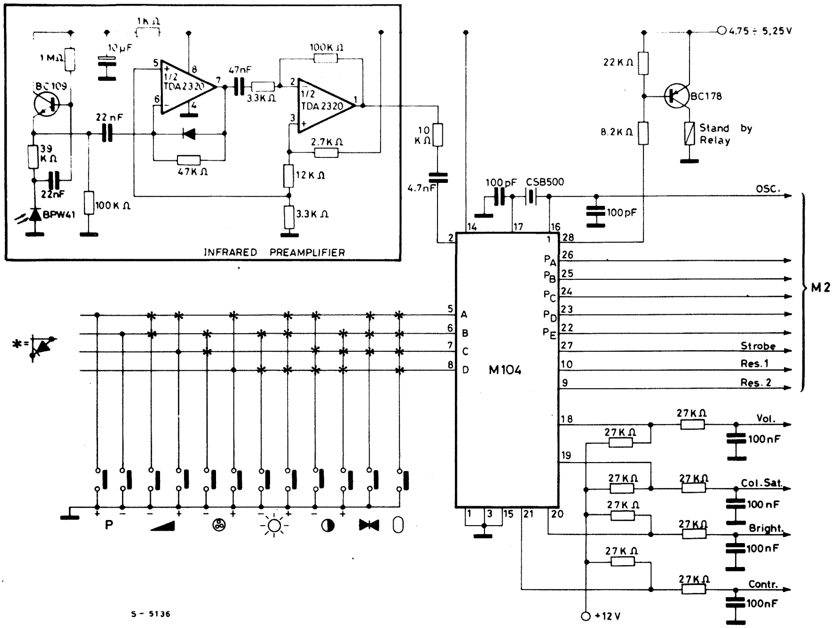


Fig. 5 - MMC II - PLL TV Frequency synthesizer



APPLICATION INFORMATION (continued)

Fig. 6 - IR Preamplifier and Remote Control receiver for 32 channel voltage synthesizer (EPM - M293)



LINEAR INTEGRATED CIRCUITS

SGS **TDA2320A**

MINIDIP STEREO PREAMPLIFIER

The TDA 2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.
The TDA 2320A is a monolithic integrated circuit in a 8 lead minidip which features:

- Wide supply voltage range (3 to 36V)
- Single or split supply operation
- Very low current consumption (0.8 mA)
- Very low distortion
- No pop-noise
- Short circuit protection

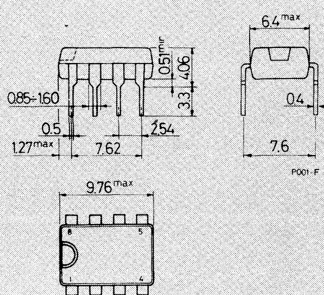
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
P_{tot}.	Total power dissipation at $T_{amb} = 70°C$	400	mW
$T_{stg,\, j}$	Storage and junction temperature	-40 to 150	°C

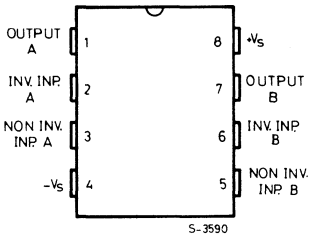
ORDERING NUMBER: TDA 2320A

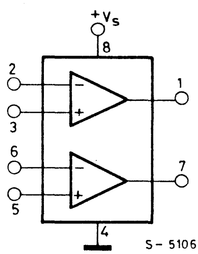
MECHANICAL DATA

Dimensions in mm

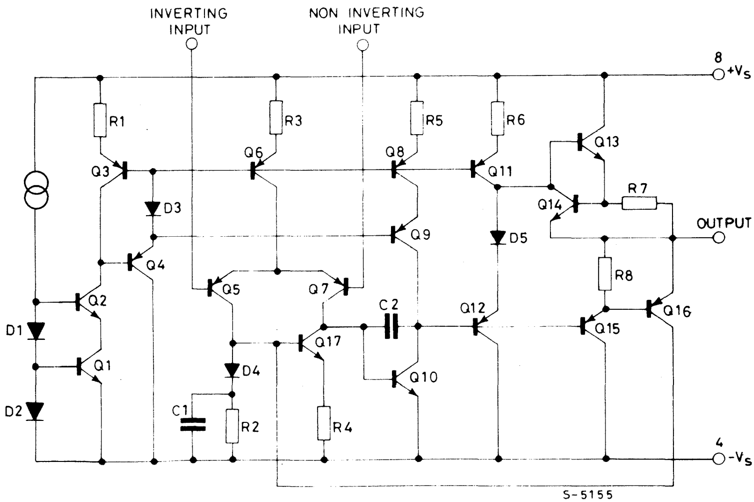


CONNECTION AND BLOCK DIAGRAM
(top view)



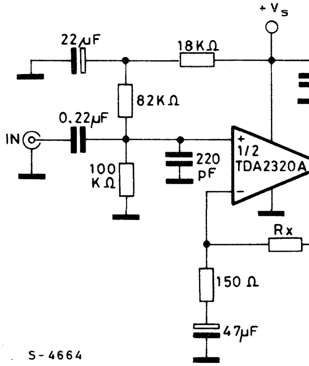


SCHEMATIC DIAGRAM
(one section)



TEST CIRCUITS

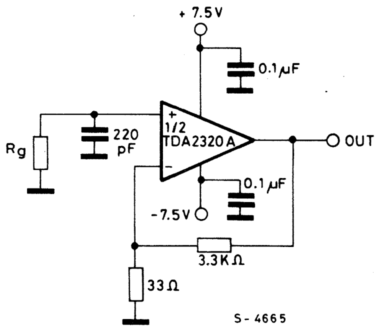
Fig. 1



$$G_v = \frac{R_x + 150}{150}$$

G_v = 20 dB for R_x = 1350Ω

Fig. 2



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage (*)			3		36	V
I_s	Supply current (*)				0.8	2	mA
I_b	Input bias current				150	500	nA
V_{os}	Input offset voltage	R_g < 10 KΩ			0.5	5	mV
I_{os}	Input offset current				10	50	nA
G_v	Open loop voltage gain	V_s = 15V	f = 333 Hz		80		dB
			f = 1 KHz		70		
			f = 10 KHz		50		
		V_s = 4.5V	f = 1 KHz		70		
V_o	Output voltage swing (*)	f = 1 KHz, R_L = 600Ω	V_s = 15V		13		Vpp
			V_s = 4.5V		2.5		
B	Gain-bandwidth product	f = 20 KHz		1.5	2.5		MHz
BW	Power bandwidth (*)	V_o = 5 Vpp, d = 1%		40	70		KHz
SR	Slew rate (*)			1	1.6		V/µS
d	Distortion (*)	V_o = 2V, G_V = 20 dB	f = 1 KHz		0.03		%
			f = 10 KHz		0.08		
e_N	Total input noise voltage (**)	Curve A	R_g = 50Ω		1		µV
			R_g = 600Ω		1.1	1.4	
			R_g = 5 KΩ		1.5		
		B = 22 Hz to 22 KHz	R_g = 50Ω		1.3		µV
			R_g = 600Ω		1.5		
			R_g = 5 KΩ		2		
		f = 1 KHz	R_g = 600Ω		9		nV/$\sqrt{Hz}$
Cs	Channel separation (**)		f = 1 KHz		100		dB
SVR	Supply voltage (**) rejection		f = 100 Hz		80		dB

(*) Test circuit of fig. 1.
(**) Test circuit of fig. 2.

Fig. 3 - Supply current vs. supply voltage

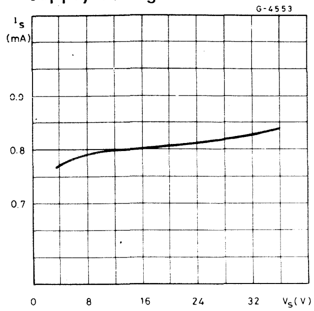


Fig. 4 - Supply current vs. ambient temperature

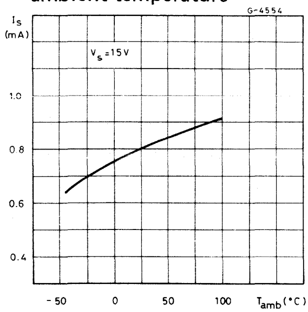


Fig. 5 - Output voltage swing vs. load resistance

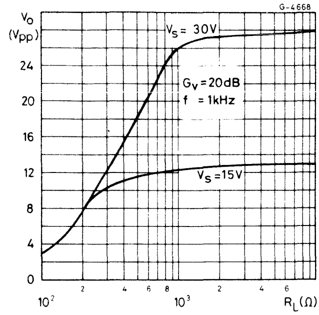


Fig. 6 - Power bandwidth

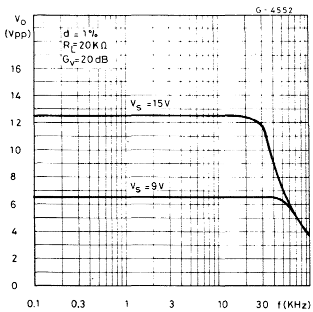


Fig. 7 - Total harmonic distortion vs. output voltage

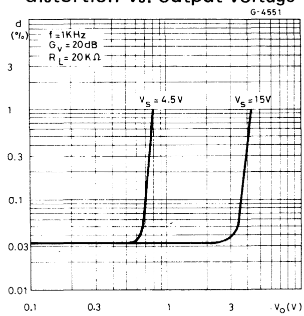


Fig. 8 - Total input noise vs. source resistance

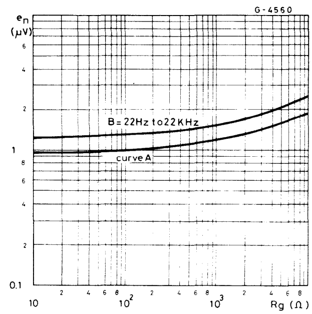


Fig. 9 - Noise density vs. frequency

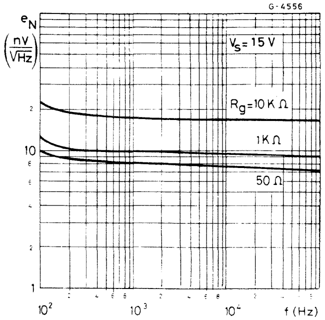


Fig. 10 - RIAA preamplifier response (circuit of fig. 12)

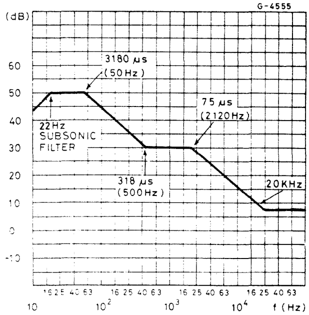
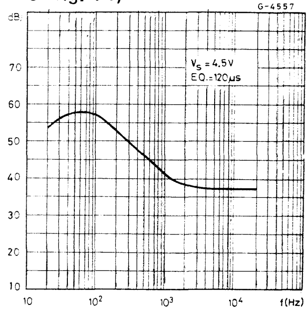


Fig. 11 - Tape preamplifier frequency response (circuit of fig. 14)



APPLICATION INFORMATION

Fig. 12 - Stereo RIAA preamplifier

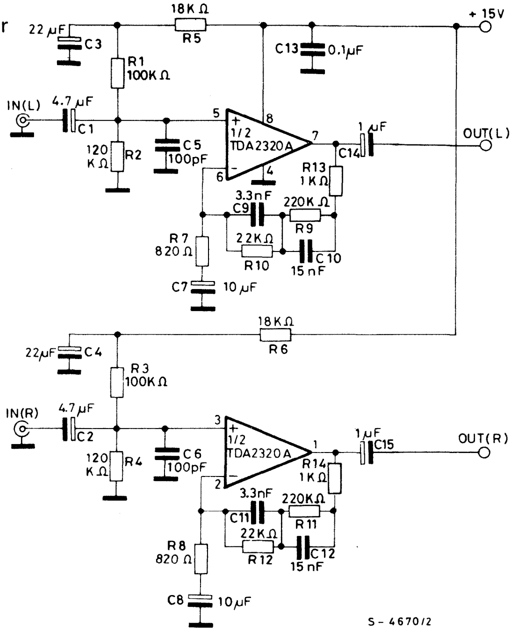
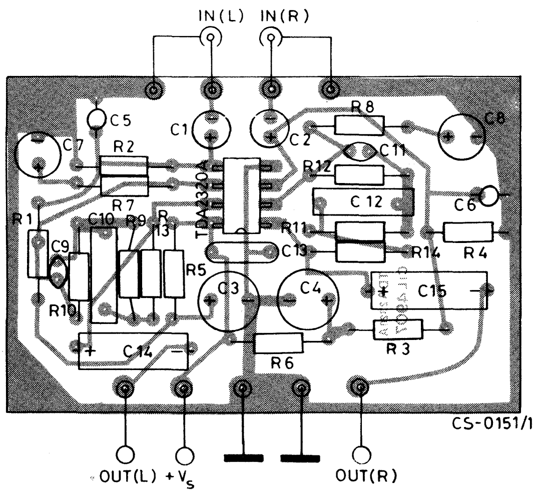


Fig. 13 - P.C. board and components layout of the circuit of fig. 12



APPLICATION INFORMATION (continued)

Fig. 14 - Stereo preamplifier for Walkman cassette players

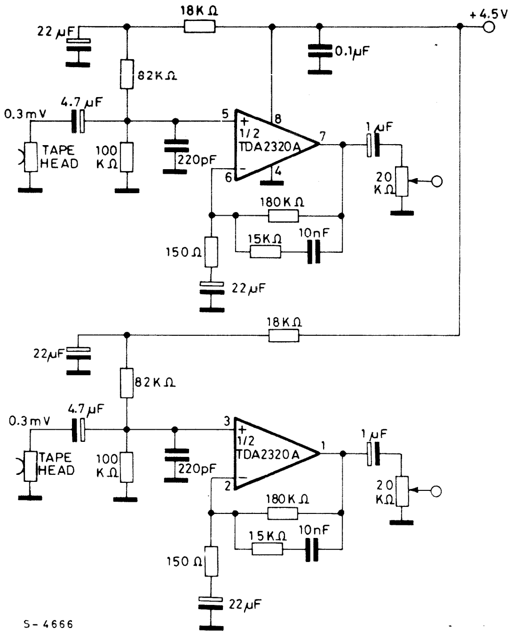


Fig. 15 - Second order 2 KHz Butterworth crossover filter for Hi-Fi active boxes

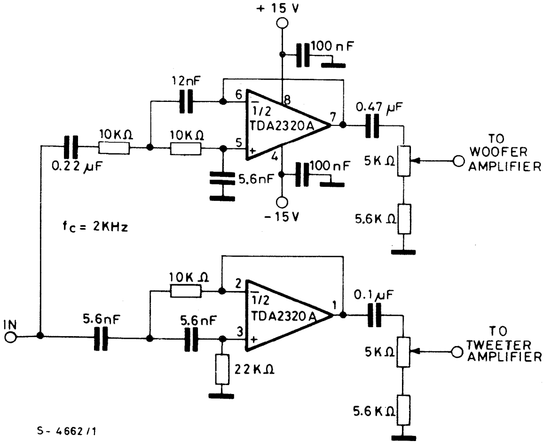
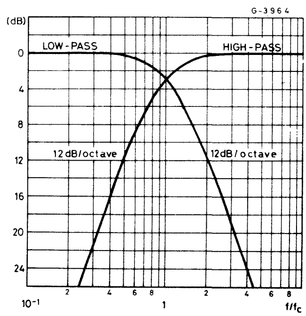


Fig. 16 - Frequency response (circuit of fig. 15)



APPLICATION INFORMATION (continued)

Fig. 17 - Third order 2.8 KHz Bessel crossover filter for Hi-Fi active boxes

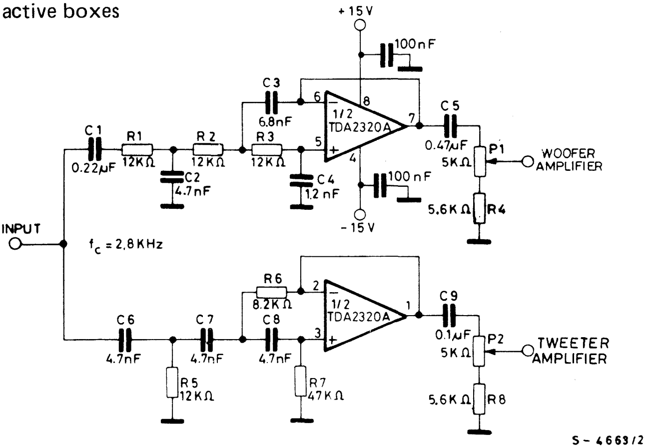


Fig. 18 - Frequency response (circuit of fig. 17)

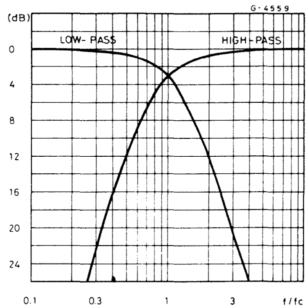


Fig. 19 - 200 Hz to 2 KHz Active Bandpass Filter for midrange speakers

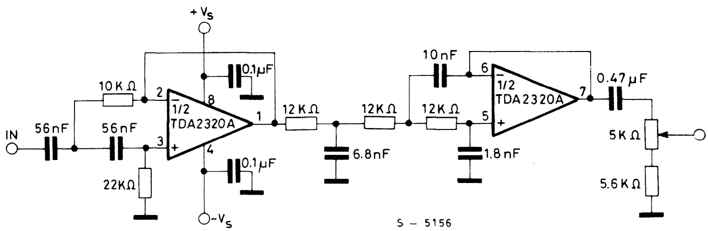
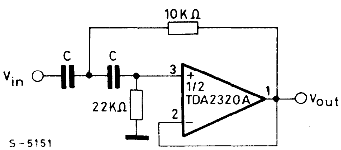
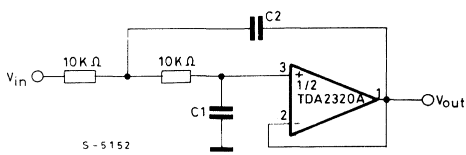


Fig. 20 - Subsonic or rumble filter



f_c (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

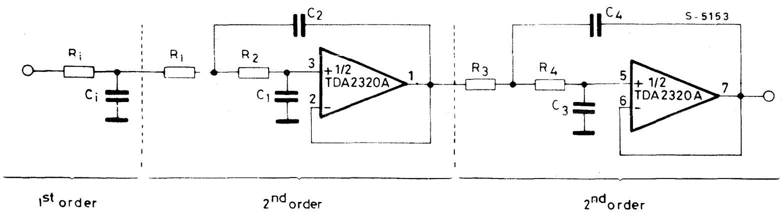
Fig. 21 - High-cut filter



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 22 - Fifth order 3.4 KHz low-pass Butterworth filter



For $f_c = 3.4$ KHz and $R_i = R1 = R2 = R3 = R4 = 10\ K\Omega$, we obtain:

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

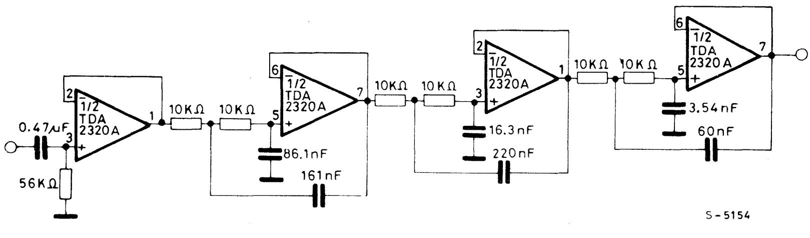
$$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 23 - Sixth-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

APPLICATION INFORMATION (continued)

Fig. 24 - Three band tone control

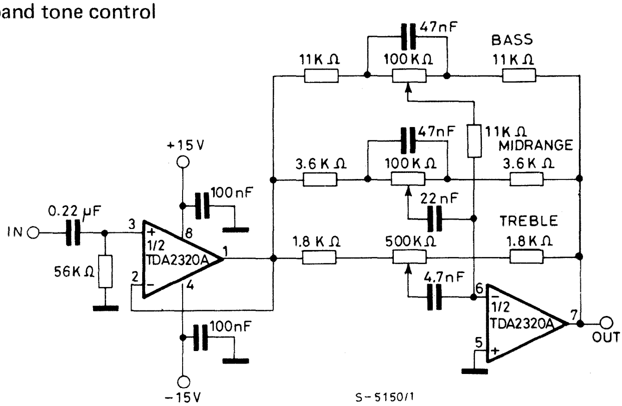
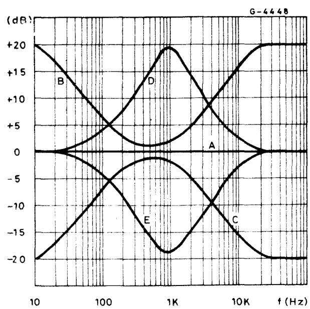


Fig. 25 - Frequency response of the circuit of fig. 24.

A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat



ULN2001A ULN2002A
ULN2003A ULN2004A

LINEAR INTEGRATED CIRCUITS

DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA peak)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The ULN2001A, ULN2002A, ULN2003A and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

ULN 2001A	General purpose, DTL, TTL, PMOS, CMOS
ULN 2002A	14-25V PMOS
ULN 2003A	5V TTL, CMOS
ULN 2004A	6 - 15V CMOS, PMOS

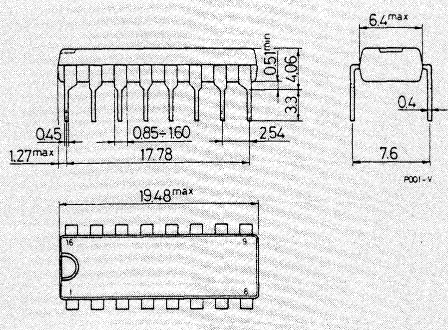
These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.
The ULN2001A/2002A/2003A and ULN2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.

ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULN2002A/2003A/2004A)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
P_{tot}	Power dissipation at $T_{amb} = 25°C$ (one Darlington pair)	1	W
	(total package)	2	W
T_{amb}	Operating ambient temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

MECHANICAL DATA

Dimensions in mm



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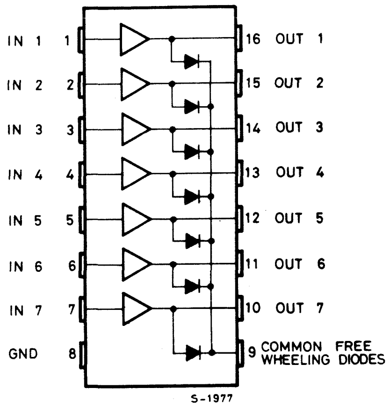
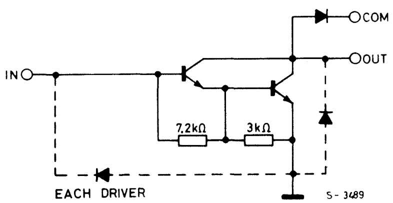
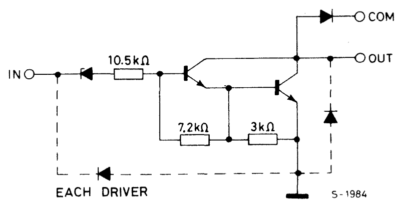
CONNECTION DIAGRAM



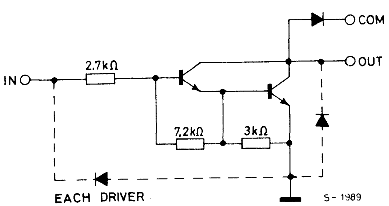
SCHEMATIC DIAGRAM



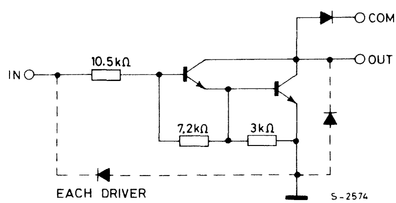
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

	Parameter	Test conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V				50	μA	1a
		T_{amb} = 70°C	V_{CE} = 50V			100	μA	1a
		T_{amb} = 70°C for **ULN2002A**						
		V_{CE} = 50V	V_i = 6V			500	μA	1b
		for **ULN2004A**						
		V_{CE} = 50V	V_i = 1V			500	μA	1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100mA	I_B = 250 μA		0.9	1.1	V	2
		I_C = 200mA	I_B = 350 μA		1.1	1.3	V	2
		I_C = 350mA	I_B = 500 μA		1.3	1.6	V	2
$I_{i(on)}$	Input current	for **ULN2002A**	V_i = 17V		0.82	1.25	mA	3
		for **ULN2003A**	V_i = 3.85V		0.93	1.35	mA	3
		for **ULN2004A**	V_i = 5V		0.35	0.5	mA	3
		V_i = 12V			1	1.45	mA	3
$I_{i(off)}$	Input current	T_{amb} = 70°C	I_C = 500 μA	50	65		μA	4
$V_{i(on)}$	Input voltage	for **ULN2002A**						
		V_{CE} = 2V	I_C = 300 mA			13	V	5
		for **ULN2003A**						
		V_{CE} = 2V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2V	I_C = 300 mA			3	V	5
		for **ULN2004A**						
		V_{CE} = 2V	I_C = 125 mA			5	V	5
		V_{CE} = 2V	I_C = 200 mA			6	V	5
		V_{CE} = 2V	I_C = 275 mA			7	V	5
		V_{CE} = 2V	I_C = 350 mA			8	V	5
h_{FE}	DC forward current gain	for **ULN2001A**						
		V_{CE} = 2V	I_C = 350 mA	1000			–	2
C_i	Input capacitance				15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o			0.25	1	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o			0.25	1	μs	–
I_R	Clamp diode leakage current	V_R = 50V				50	μA	6
		T_{amb} = 70°C	V_R = 50V			100	μA	6
V_F	Clamp diode forward voltage	I_F = 350 mA			1.7	2	V	7

TEST CIRCUITS

Fig. 1a

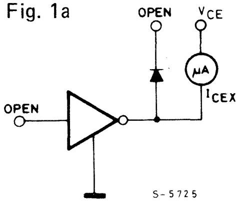


Fig. 1b

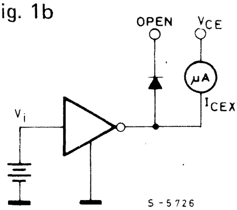


Fig. 2

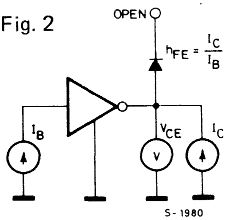


Fig. 3

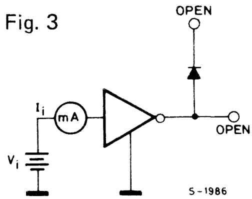


Fig. 4

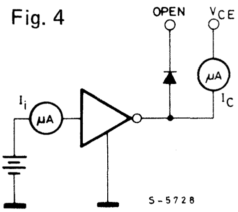


Fig. 5

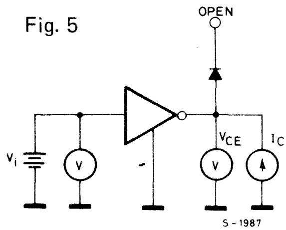


Fig. 6

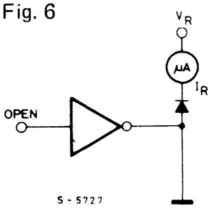
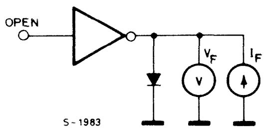


Fig. 7



LINEAR INTEGRATED CIRCUITS

SGS ULN2064B/2066B ULN2068B/2070B ULN2074B/2076B

50V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V.
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B AND ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES
- 16-pin POWERDIP PACKAGE

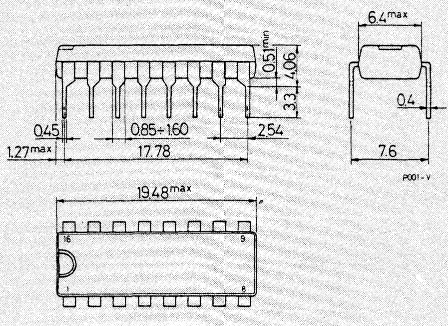
Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four darlington switches delivering up to 1.5A with a specified minimum breakdown of 50V and a sustaining voltage of 35V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5V logic families and the ULN2066B and ULN2076B are compatible with 6-15V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic. All of these arrays are supplied in a 16-pin powerdip package with the four center pins used to conduct heat to the printed circuit copper.

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage		50	V
$V_{CE(sus)}$	Output sustaining voltage		35	V
I_o	Output current		1.75	A
V_i	Input voltage	for ULN2066B/70B/74B/76B	30	V
		for ULN2064B/68B	15	V
I_i	Input current		25	mA
V_s	Supply voltage	for ULN2068B	10	V
		for ULN2070B	20	V
P_{tot}	Power dissipation:	at $T_{pins} = 90°C$	4.3	W
		at $T_{amb} = 70°C$	1	W
T_{amb}	Operating ambient temperature range		-20 to 85	°C
T_{stg}	Storage temperature		-55 to 150	°C

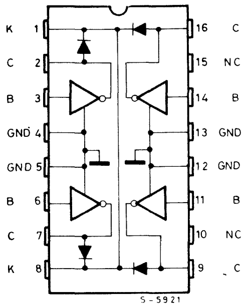
MECHANICAL DATA

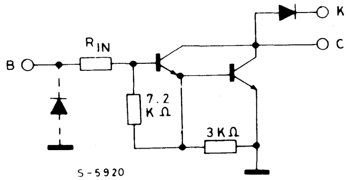
Dimensions in mm



ULN2064B/2066B ULN2068B/2070B ULN2074B/2076B

CONNECTION AND SCHEMATIC DIAGRAMS



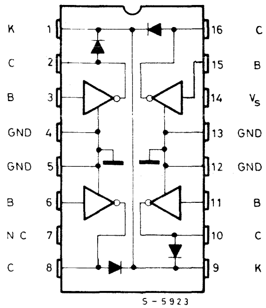


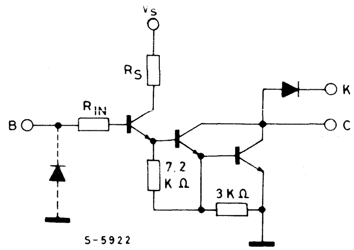
ULN2064B : R_{IN} = 350Ω
ULN2066B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2064B-ULN2066B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2064B-ULN2066B** I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625μA I_C = 750mA I_B = 935μA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$	Input current	for **ULN2064B** V_i = 2.4V for **ULN2064B** V_i = 3.75V for **ULN2066B** V_i = 5V for **ULN2066B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2064B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2066B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	μs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	μs	
I_R	Clamp diode leakage current	for **ULN2064B-ULN2066B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 μA μA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

CONNECTION AND SCHEMATIC DIAGRAMS



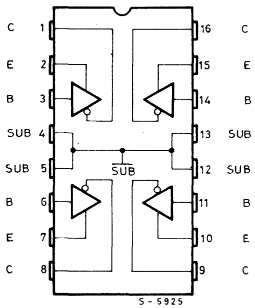


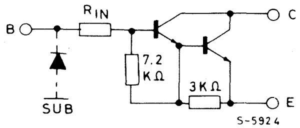
ULN2068B : R_{IN} = 2.5 kΩ R_s = 900Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5V for ULN2068B, V_s = 12V for ULN2070B, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2068B-ULN2070B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2068B-ULN2070B** I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	for **ULN2068B** I_C = 500 mA V_i = 2.75V I_C = 750mA V_i = 2.75V I_C = 1A V_i = 2.75V I_C = 1.25A V_i = 2.75V for **ULN2070B** I_C = 500mA V_i = 5V I_C = 750mA V_i = 5V I_C = 1A V_i = 5V I_C = 1.25A V_i = 5V			 1.1 1.2 1.3 1.4 1.1 1.2 1.3 1.4	 V V V V V V V V	2
$I_{i(on)}$	Input current	for **ULN2068B** V_i = 2.75V for **ULN2068B** V_i = 3.75V for **ULN2070B** V_i = 5V for **ULN2070B** V_i = 12V			550 1000 400 1250	µA µA µA µA	4
$V_{i(on)}$	Input voltage	V_{CE} = 2V I_C = 1.5A for **ULN2068B** for **ULN2070B**			 2.75 5	 V V	5
I_s	Supply current	for **ULN2068B** I_C = 500mA V_i = 2.75V for **ULN2070B** I_C = 500mA V_i = 5V			 6 4.5	 mA mA	8
t_{PLH}	Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	µs	
t_{PHL}	Turn-off delay time	$0.5V_i$ to $0.5V_o$ I_C = 1.25A			1.5	µs	
I_R	Clamp diode leakage current	for **ULN2068B-ULN2070B** V_R = 50V V_R = 50V T_{amb} = 70°C			 50 100	 µA µA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

CONNECTION AND SCHEMATIC DIAGRAMS





ULN2074B : R_{IN} = 350Ω
ULN2076B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2074B-ULN2076B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2074B-ULN2076B** I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$	Input current	for **ULN2074B** V_i = 2.4V for **ULN2074B** V_i = 3.75V for **ULN2076B** V_i = 5V for **ULN2076B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2074B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2076B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	µs	
t_{PHL}	Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	µs	

TEST CIRCUITS

Fig. 1

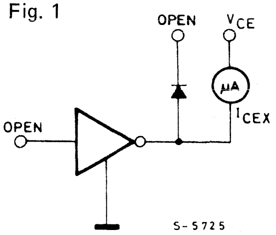


Fig. 2

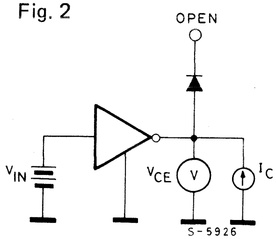


Fig. 3

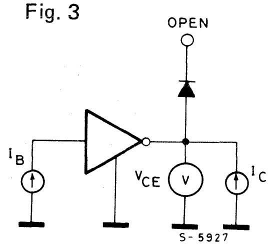


Fig. 4

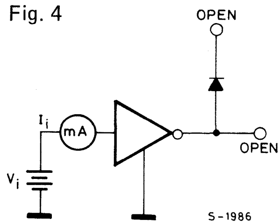


Fig. 5

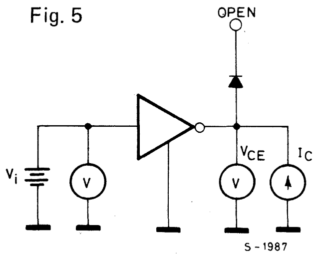


Fig. 6

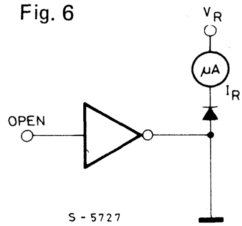


Fig. 7

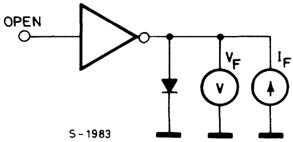


Fig. 8

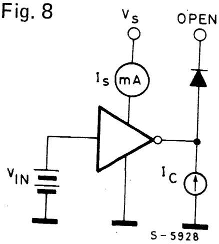


Fig. 9 - Input current as a function of input voltage

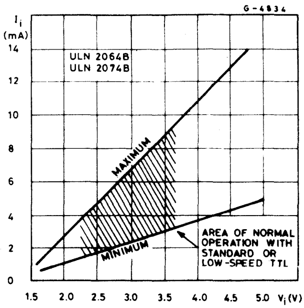


Fig. 10 - Input current as a function of input voltage

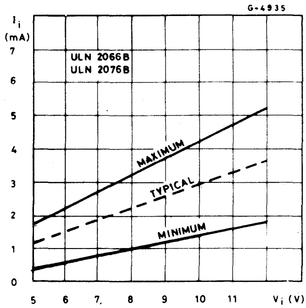
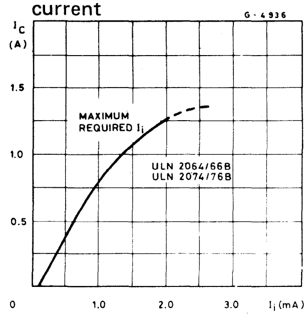


Fig. 11 - Collector current as a function of input current



TYPICAL APPLICATIONS

Fig. 12 - Common-anode LED drivers

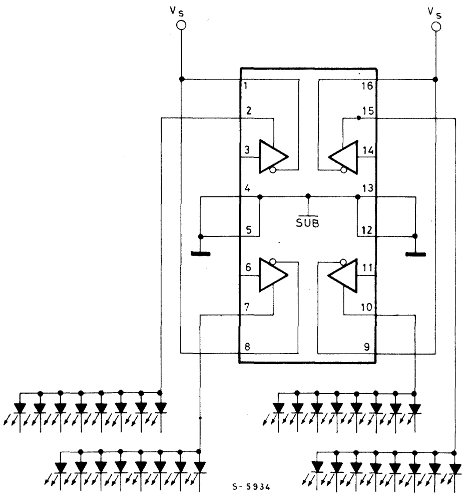
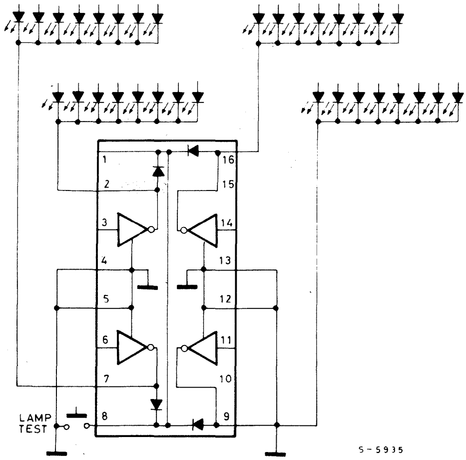


Fig. 13 - Common-cathode LED drivers



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).
The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 14 - Example of P.C. board copper area which is used as heatsink.

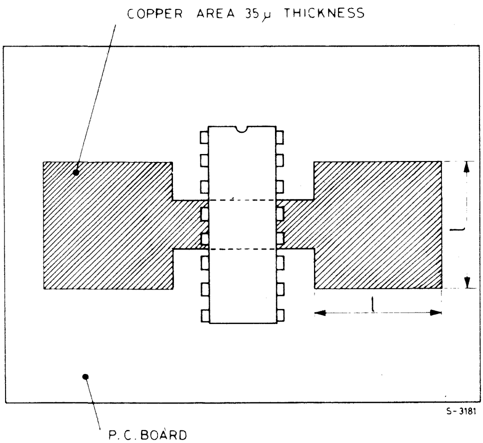


Fig. 15 - External heatsink mouting example

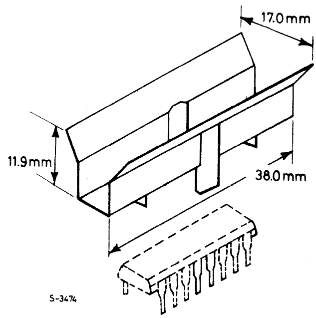


Fig. 16 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

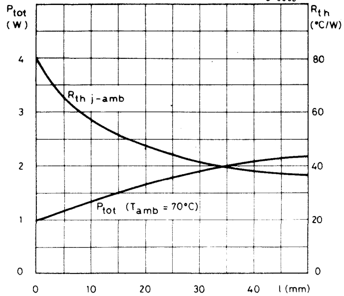
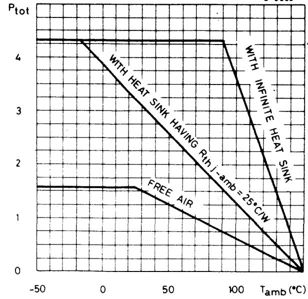


Fig. 17 - Maximum allowable power dissipation vs. ambient temperature



ULN2065B/2067B
ULN2069B/2071B
ULN2075B/2077B

LINEAR INTEGRATED CIRCUITS

80V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B AND ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B AND ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES
- 16-pin POWERDIP PACKAGE

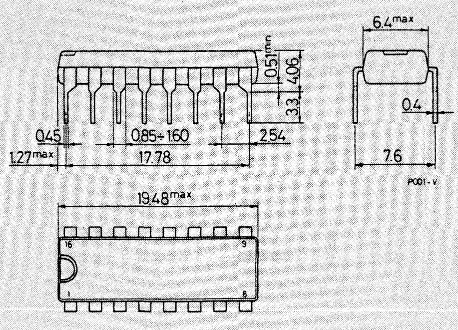
Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four darlington switches delivering up to 1.5A with a specified minimum breakdown of 80V and a sustaining voltage of 50V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15V CMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic. All of these arrays are supplied in a 16-pin powerdip, package with the four center pins used to conduct heat to the PCB copper.

ABSOLUTE MAXIMUM RATINGS

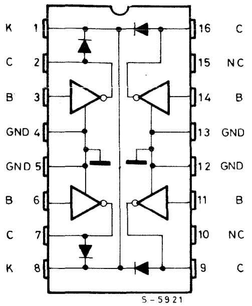
V_{CEX}	Output voltage	80	V
$V_{CE(sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage for ULN2075B - 2077B	60	V
	for ULN2067B - 2071B	30	V
	for ULN2065B - 2069B	15	V
I_i	Input current	25	mA
V_s	Supply voltage for ULN2069B	10	V
	for ULN2071B	20	V
P_{tot}	Power dissipation: at $T_{pins} = 90°C$	4.3	W
	at $T_{amb} = 70°C$	1	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature	-55 to 150	°C

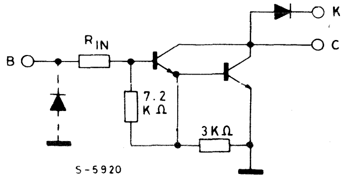
MECHANICAL DATA

Dimensions in mm



CONNECTION AND SCHEMATIC DIAGRAMS





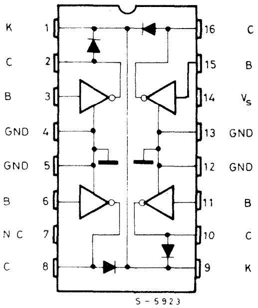
ULN2065B : R_{IN} = 350Ω
ULN2067B : R_{IN} = 3 kΩ

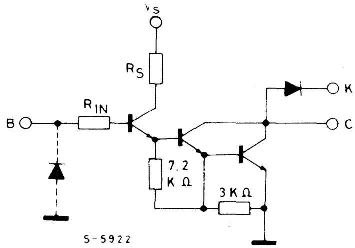
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2065B-ULN2067B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2065B-ULN2067B** I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625μA I_C = 750mA I_B = 935μA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA for **ULN2065B-ULN2067B** I_C = 1.5A I_B = 2.25mA			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$	Input current	for **ULN2065B** V_i = 2.4V for **ULN2065B** V_i = 3.75V for **ULN2067B** V_i = 5V for **ULN2067B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2065B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2067B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL}	Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	
I_R	Clamp diode leakage current	for **ULN2065B-ULN2067B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 μA μA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

ULN2065B/2067B ULN2069B/2071B ULN2075B/2077B

CONNECTION AND SCHEMATIC DIAGRAMS



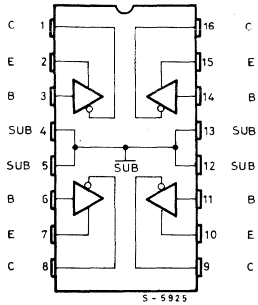


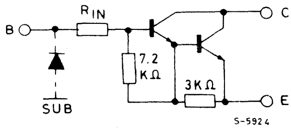
ULN2069B : R_{IN} = 2.5 kΩ, R_s = 900Ω
ULN2071B : R_{IN} = 11.6 kΩ, R_s = 3.4 kΩ

ELECTRICAL CHARACTERISTICS (V_s = 5V for ULN2069B, V_s = 12V for ULN2071B, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2069B-ULN2071B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2069B-ULN2071B** I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	for **ULN2069B** I_C = 500 mA V_i = 2.75V I_C = 750mA V_i = 2.75V I_C = 1A V_i = 2.75V I_C = 1.25A V_i = 2.75V I_C = 1.5A V_i = 2.75V for **ULN2071B** I_C = 500mA V_i = 5V I_C = 750mA V_i = 5V I_C = 1A V_i = 5V I_C = 1.25A V_i = 5V I_C = 1.5A V_i = 5V			 1.1 1.2 1.3 1.4 1.5 1.1 1.2 1.3 1.4 1.5	 V V V V V V V V V V	2
$I_{i(on)}$	Input current	for **ULN2069B** V_i = 2.75V for **ULN2069B** V_i = 3.75V for **ULN2071B** V_i = 5V for **ULN2071B** V_i = 12V			550 1000 400 1250	μA μA μA μA	4
$V_{i(on)}$	Input voltage	V_{CE} = 2V I_C = 1.5A for **ULN2069B** for **ULN2071B**			 2.75 5	V	5
I_s	Supply current	for **ULN2069B** I_C = 500mA V_i = 2.75V for **ULN2071B** I_C = 500mA V_i = 5V			 6 4.5	 mA mA	8
t_{PLH}	Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL}	Turn-off delay time	$0.5V_i$ to $0.5V_o$ I_C = 1.25A			1.5	μs	
I_R	Clamp diode leakage current	for **ULN2069B-ULN2071B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 μA μA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

CONNECTION AND SCHEMATIC DIAGRAMS





ULN2075B : R_{IN} = 350Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2075B-ULN2077B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2075B-ULN2077B** I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625μA I_C = 750mA I_B = 935μA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA for **ULN2075B-ULN2077B** I_C = 1.5A I_B = 2.25mA			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$	Input current	for **ULN2075B** V_i = 2.4V for **ULN2075B** V_i = 3.75V for **ULN2077B** V_i = 5V for **ULN2077B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2075B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2077B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL}	Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	

TEST CIRCUITS

Fig. 1

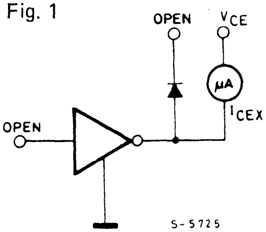


Fig. 2

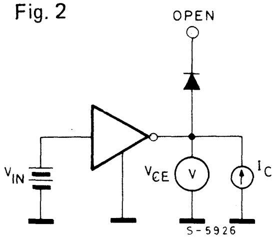


Fig. 3

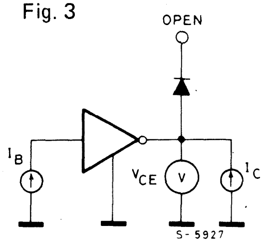


Fig. 4

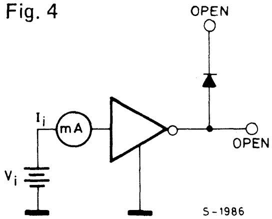


Fig. 5

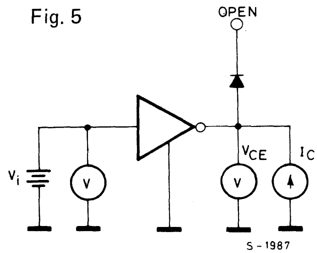


Fig. 6

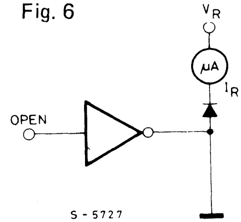


Fig. 7

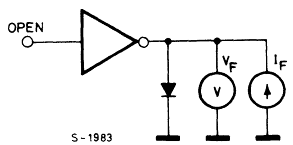


Fig. 8

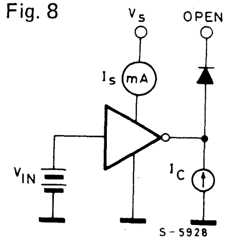


Fig. 9 - Input current as a function of input voltage

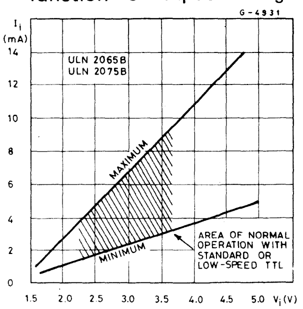


Fig. 10 - Input current as a function of input voltage

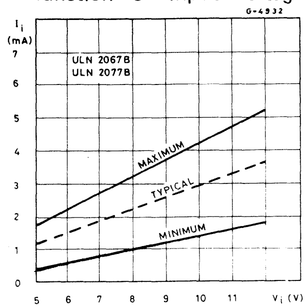
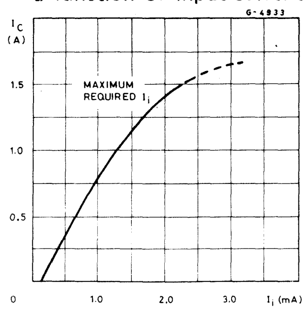


Fig. 11 - Collector current as a function of input current



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).
The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area which is used as heatsink.

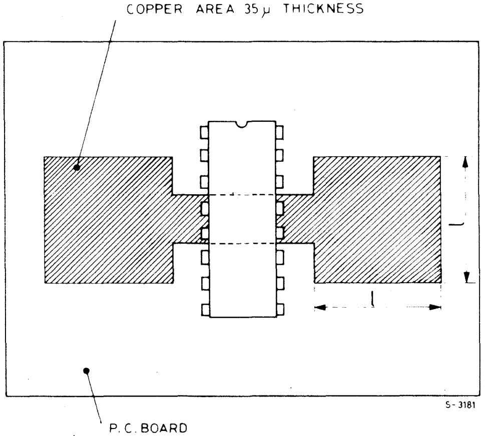


Fig.13 - External heatsink mounting example

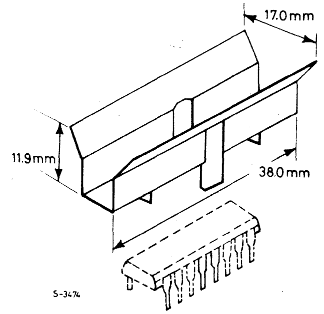


Fig. 14 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

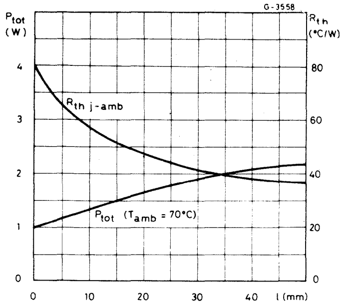
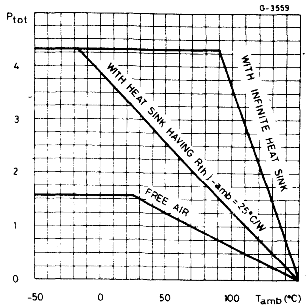


Fig. 15 - Maximum allowable power dissipation vs. ambient temperature



ULN2801A/2802A
ULN2803A/2804A
ULN2805A

LINEAR INTEGRATED CIRCUITS

DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA (600 mA peak)
- OUTPUT VOLTAGE TO 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUTS CAN BE PARALLELED OR HIGHER CURRENT
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

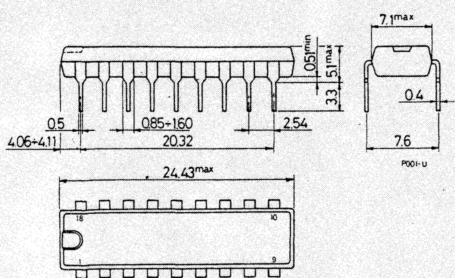
The ULN2801A - ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.
Five versions are available to simplify interfacing to standard logic families: the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5 KΩ input resistor and zener for 14-25V PMOS; the ULN2803A has a 2.7 KΩ input resistor for 5V TTL and CMOS; the ULN2804A has a 10.5 KΩ input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.
All types are supplied in an 18-lead plastic DIP with a copper lead frome and feature the convenient input-opposite-output pinout to simplify board layout.

ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_i	Input voltage for ULN 2802A, 2803A, 2804A	30	V
	for ULN 2805A	15	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_{tot}	Power dissipation (one Darlington pair)	1.0	W
	(total package)	2.25	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

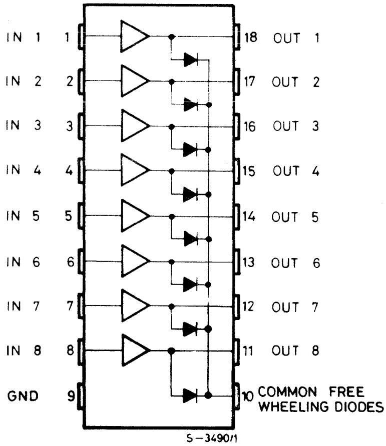
MECHANICAL DATA

Dimensions in mm



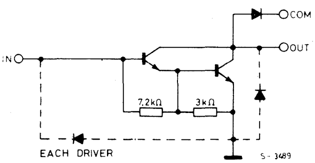
CONNECTION DIAGRAM

(top view)

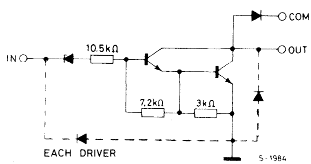


SCHEMATIC DIAGRAMS

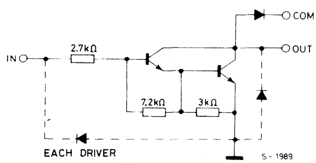
For ULN 2801A (each driver for PMOS-CMOS)



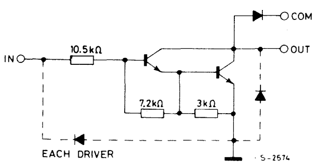
For ULN 2802A (each driver for 14-15V PMOS)



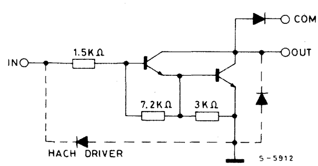
For ULN 2803A (each driver for 5V, TTL/CMOS)



For ULN 2804A (each driver for 6-15V CMOS/PMOS)



For ULN 2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE}= 50V T_{amb}= 70°C V_{CE}= 50V T_{amb}= 70°C for **ULN 2802A** V_{CE}= 50V V_i = 6V for **ULN 2804A** V_{CE}= 50V V_i = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100 mA I_B = 250 µA I_C = 200 mA I_B = 350 µA I_C = 350 mA I_B = 500 µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
$I_{i(on)}$	Input current	for **ULN 2802A** V_i = 17V for **ULN 2803A** V_i = 3.85V for **ULN 2804A** V_i = 5V V_i = 12V for **ULN 2805A** V_i = 3V		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
$I_{i(off)}$	Input current	T_{amb}= 70°C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input voltage	for **ULN 2802A** V_{CE}= 2V I_C = 300 mA for **ULN 2803A** V_{CE}= 2V I_C = 200 mA V_{CE}= 2V I_C = 250 mA V_{CE}= 2V I_C = 300 mA for **ULN 2804A** V_{CE}= 2V I_C = 125 mA V_{CE}= 2V I_C = 200 mA V_{CE}= 2V I_C = 275 mA V_{CE}= 2V I_C = 350 mA for **ULN 2805A** V_{CE}= 2V I_C = 350 mA			 13 2.4 2.7 3 5 6 7 8 2.4	 V V V V V V V V V	5
h_{FE}	DC forward current gain	for **ULN 2801A** V_{CE}= 2V I_C = 350 mA	1000			–	2
C_i	Input capacitance			15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp diode leakage current	V_R = 50V T_{amb}= 70°C V_R = 50V			50 100	µA µA	6
V_F	Clamp diode forward voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Fig. 1a

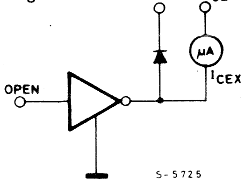


Fig. 1b

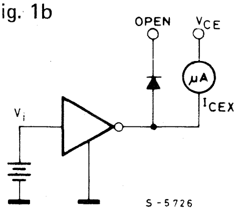


Fig. 2

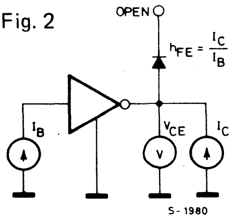


Fig. 3

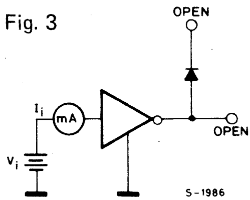


Fig. 4

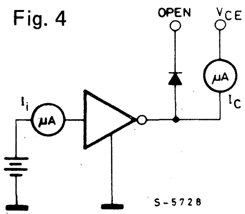


Fig. 5

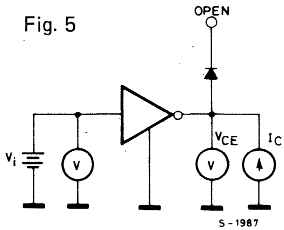


Fig. 6

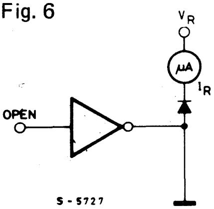
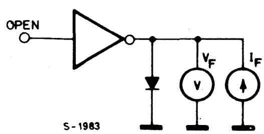


Fig. 7



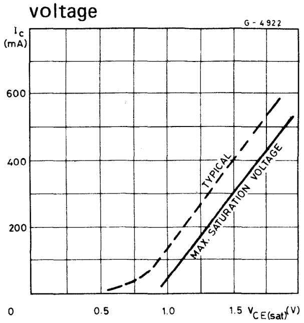


Fig. 8 - Collector current as a function of saturation voltage

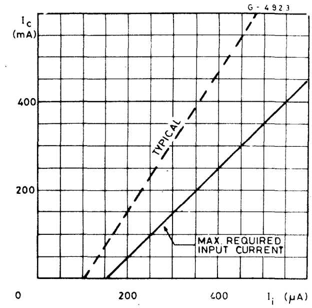


Fig. 9 - Collector current as a function of input current

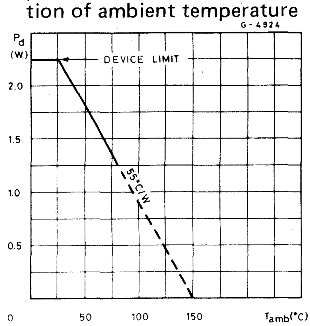


Fig. 10 - Allowable average power dissipation as a function of ambient temperature

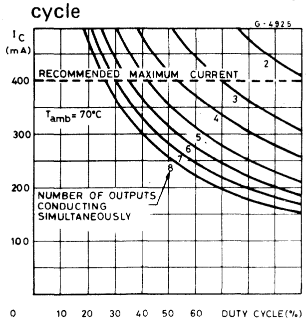


Fig. 11 - Peak collector current as a function of duty cycle

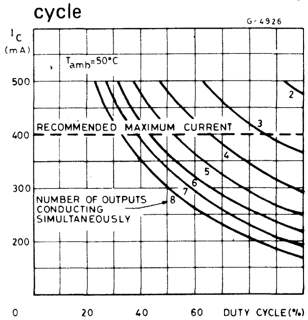


Fig. 12 - Peak collector current as a function of duty cycle

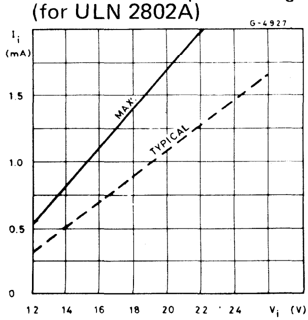


Fig. 13 - Input current as a function of input voltage (for ULN 2802A)

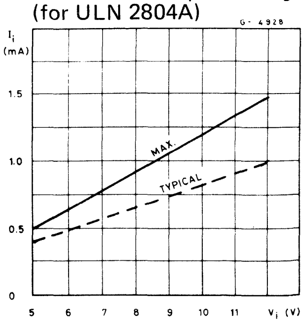


Fig. 14 - Input current as a function of input voltage (for ULN 2804A)

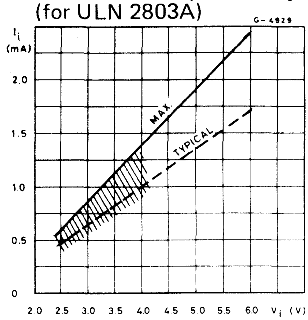


Fig. 15 - Input current as a function of input voltage (for ULN 2803A)

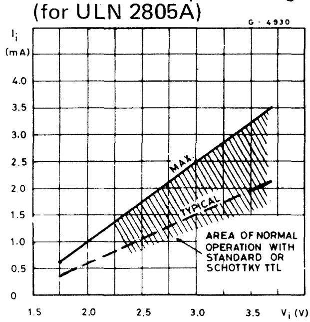


Fig. 16 - Input current as a function of input voltage (for ULN 2805A)

OTHER BIPOLAR CIRCUITS

Industrial Circuits

LINEAR DRIVERS

TYPE	FUNCTION	DESCRIPTION	PACKAGE
L149	4A Linear Driver	Push-pull current booster delivering to 4A with current gain typically 10000. Operates at up to 40V and features 30V/μs slew rate.	Pentawatt®
L165	Power op. amp.	3A power op.. amp. with supply voltage 36V and slew rate of 8V/μs. Inputs are ground compatible and device is SOA protected.	Pentawatt®
L465 A	Power op. amp.	3.5A high efficiency power op. amp. with supply voltage to 36V and slew rate of 14V/μs. Inputs are ground compatible and device is SOA protected.	Pentawatt®
L272	Dual power op. amp.	Two 1.5A/28V power op. amps for DC motor driving/power-supply applications. Features low saturation, ground compatible inputs plus large common-mode and differential mode range.	16-pin DIP
L272M	Dual power op. amp.	Same as L272 except packaged in Minidip for applications where dissipation is lower.	Minidip

SWITCHMODE DRIVERS

TYPE	FUNCTION	DESCRIPTION	PACKAGE
L292	Switchmode DC motor driver	Output current, regulated by internal PWM chopper, proportional to input voltage. Delivers up to 2A at 36V with bridge output stage. With L290 and L291 forms complete DC motor servopositioning system.	Multiwatt® 15
L294	Switchmode solenoid driver	Controlled by TTL compatible logic input, delivers 4A at 50V to drive high speed solenoids. Current regulated by constant ripple PWM chopper and externally adjustable. Features latched diagnostic output and protection circuits.	Multiwatt® 15
L295	Dual Switchmode Driver	Two 50V/2.5A switchmode drivers controlled by TTL - compatible logic inputs. Current regulated by constant frequency PWM circuit and externally adjustable.	Multiwatt® 15

BRIDGE DRIVERS

TYPE	FUNCTION	DESCRIPTION	PACKAGE
L293	Quad Push-Pull Driver	Four 1A/36V push-pull drivers for use singly or as two bridges. Each driver controlled by logic input; each bridge controlled by enable input. Connects directly to low level logic.	16-pin DIP
L293E	Quad Push-Pull Driver	Same as L293 plus external emitter connections to each driver for load current sensing.	20-pin DIP
L298	Dual Bridge Driver	Four 2A/50V push-pull drivers for use as two bridges. Each driver controlled by logic input; each bridge controlled by enable input. External connections to each bridge for load currents sensing. Connects directly to low level logic.	Multiwatt® 15

SPECIAL FUNCTIONS

TYPE	FUNCTION	DESCRIPTION	PACKAGE
L290	Tachometer converter	Processes signals from optical encoder to give tacho and position outputs. Also generates reference voltage and pulse outputs. With L291 and L292 form 3-chip DC motor servopositioning system.	16-pin DIP
L291	D/A converter and error amplifier	Contains 5-bit D/A converter with switchable polarity, error amplifier and position amplifier. With L290 and L293 forms complete 3-chip DC motor servopositioning system.	16-pin DIP
L297	Stepper motor controller	Contains translator plus PWM choppers for two-phase bipolar and four-phase unipolar PM motors. Driven by step clock and direction inputs and generates normal, wave drive and half step sequences. With L293E or L298 forms complete bipolar step motor interface.	20-pin DIP
L297A	Stepper motor controller	As L297A plus pulse doubler on step clock input for double stepping.	20-pin DIP

Industrial Circuits

SPECIAL FUNCTIONS (continued)

TYPE	FUNCTION	DESCRIPTION	PACKAGE
L3654	Printer solenoid driver	Ten bit SIPO shift register with open collector outputs handling 250 mA each at up to 45V. Serial output allows cascading without limit.	16-pin DIP
L5832	Solenoid controller	With one or two external darlingtons drives solenoids efficiently with PWM regulated current. Can provide single or two level current waveforms and the waveshape is externally adjustable.	16-pin DIP
L120A	Triac/SCR Phase control	For use as phase controller in industrial and consumer applications.	16-pin DIP
L121A	Triac/SCR Burst control	For use as burst controller in industrial and consumer applications.	16-pin DIP

DARLINGTON ARRAYS

TYPE	DESCRIPTION	V_{CEX}	I_o (each)	PACKAGE
L201, L202, L203, L204	Seven NPN darlingtons with common emitters and suppression diodes	50V	500 mA	16-pin DIP
L601, L602, L603, L604	Eight NPN darlingtons with common emitters and suppression diodes	90V	400 mA	16-pin DIP
L702	Four NPN darlingtons with common emitters.	90V	2A	Powerdip 8+8 or Multiwatt-11
L7150, L7152	Four NPN darlingtons with common emitters and suppression diodes.	50V	1.5A	Multiwatt-15
L7180, L7182	Four NPN darlingtons with common emitters and suppression diodes.	80V	1.5A	Multiwatt-15

DARLINGTON ARRAYS (continued)

TYPE	DESCRIPTION	V_{CEX}	I_o (each)	PACKAGE
ULN2001A, ULN2002A, ULN2003A, ULN 2004A	Seven NPN darlingtons with common emitters and suppression diodes.	50V	500 mA	16-pin DIP
ULN2064B, ULN2065B, ULN2066B, ULN2067B	Four NPN darlingtons with common emitters and suppression diodes.	50V 80V 50V 80V	1.5A	Powerdip 12+2+2
ULN2068B, ULN2069B, ULN2070B, ULN2071B	Four NPN darlingtons with common emitters, predriver stages and suppression diodes.	50V 80V 50V 80V	1.5A	Powerdip 12 +2 +2
ULN2074B, ULN2075B, ULN2076B, ULN2077B	Four NPN darlingtons with fully isolated pinouts.	50V 80V 50V 80V	1.5A	Powerdip 12 +2 +2
ULN2801A, ULN2802A, ULN2803A, ULN2804A, ULN2805A	Eight NPN darlingtons with common emitters and suppression diodes.	50V	500 mA	18-pin DIP

Automotive Circuits

IGNITION CONTROL

TYPE	FUNCTION	FEATURES	PACKAGE
L482	Electronic ignition controller (Hall-effect pickup)	For Hall-effect pickup breakerless ignition systems. Drives an external darlington to provide regulated current in ignition coil with low power dissipation. Can also be used as dwell control section and driver stage in microprocessor-controlled systems. Includes protection against permanent conduction, overvoltage and dump transients to 120V.	16-pin DIP and Microwatt (16-pin power micropackage)
L497	Electronic ignition controller (Hall-effect pickup)	For Hall-effect pickup breakerless ignition systems. Drives an external darlington to provide regulated current in the ignition coil with low power dissipation. Can also be used as dwell control section and driver stage in microprocessor-controlled systems. Includes protection against permanent conduction, overvoltages and dump transients to 120V. Built in timer for calibrated control of dwell angle when 90% of required coil current not reached.	16-pin DIP and Microwatt (16-pin power micropackage)
L484	Electronic ignition controller (Magnetic pickup)	For breakerless ignition systems with magnetic pickup. Drives an external darlington to provide regulated current with low dissipation. Features zero crossing detection plus protection against overvoltages and dump transients to 120V. Pickup signal referred to ground. Circuit is insensitive to variations in pickup waveform.	16-pin DIP and Microwatt (16-pin power micropackage)

FUEL INJECTION

L583	Injector solenoid controller	Connected directly to control micro and driving two external darlingtons, provides high current peak to open injector then lower holding current to keep it open. Includes switchmode regulation and dump protection up to 80V.	Powerdip 12 + 2 + 2
L483	Injector solenoid driver	Connected directly to control micro, provides high current peak (4A) to open injector then lower holding current (1A) to keep it open. Includes dump protection up to 80V.	Pentawatt®

FLASHER CONTROL

TYPE	FUNCTION	FEATURES	PACKAGE
L486	Direction indicator driver	Drives flashing direction indicators in automobiles. Faults indicated by automatic speedup of flash rate. Features high current capability (1A) and dump protection to 80V.	Minidip

AUTOMOTIVE VOLTAGE REGULATORS

L487	Very low drop 5V regulator with reset	– Output current of 500 mA with 0.6V drop. – Includes reset function and ±80V dump protection.	Pentawatt®
L2600 series	Low drop fixed regulators (5, 8.5 & 10V)	– Output current of 500mA. – Include ± 100V dump protection.	Versawatt
L4700 series	Very low drop fixed regulators (5, 8.5 & 10V)	– Output current 500 mA with 0.5V drop. – Include ± 80V dump protection.	Versawatt
L4800 series	Very low drop fixed regulators (5, 8.5 & 10V)	– Output current of 400 mA with 0.4V drop. – Include ± 60V dump protection plus foldback current limiting.	Versawatt
LM 2930A	Very low drop 5V regulator	– Output current 400 mA with 0.4V drop. – Includes ± 40V dump protection and foldback current limiting.	Versawatt
LM 2931A	Very low drop 5V regulator	– Output current 400 mA with 0.4V drop. – Includes ± 60V dump protection and foldback current limiting.	Versawatt

Telecom Circuits

TELEPHONE SPEECH CIRCUITS

TYPE	FUNCTION	FEATURES	PACKAGE
LS 285	Speech circuit	Replaces hybrid circuit (2/4 wire interface) in telephones. Provides automatic gain control and works typically with dynamic transducers.	14-pin DIP
LS 288	Programmable speech circuit	Telephone speech circuit with programmable gains, automatic gain control and fixed gain operation. Suitable for both piezoceramic and dynamic transducers.	16-pin DIP
LS 156	Speech circuit with MF tone interface	Telephone speech circuit incorporating Mf interface. Automatic gain control for voice signals. Designed for piezoceramic transducers. Automatically adjusts balancing impedance to match line.	16-pin DIP
LS 356	Speech circuit with MF tone interface	Telephone speech circuit incorporating MF interface. Features automatic gain control for voice signal and fixed gain mode. Used typically with dynamic transducers but a small loudspeakers can be used for receiver thanks to high current available at output.	16-pin DIP
LS 656	Speech circuit with MF tone interface and low drop	Same as LS356 plus low voltage drop.	16-pin DIP
LS 348	Fully programmable speech circuit	Telephone speech circuit with adjustable gains, AGC current thereshold and AGC range. Can work with both dynamic and piezoceramic transducers and the voltage drop is particularly low. Can be set to standby state, consuming very little current but still matching AC & DC impedances to line.	20-pin DIP
LS 388	Low consumption speech circuit	Telephone speech circuit with programmable gains, automatic gain control and fixed gain operation. Both send and receive gains can be set to very high levels. Special features include low voltage drop and very low current consumption.	16-pin DIP

OTHER TELECOM CIRCUITS

TYPE	FUNCTION	FEATURES	PACKAGE
LS 188	Microphone preamplifier	Designed for use with a magnetic or piezo-ceramic transducer to replace carbon microphone in conventional telephones. Pin-programmable gain.	Minidip
LS 1240	Electronic two-tone ringer	Replaces mechanical bell in telephones. Features include low current consumption, integrated rectifier bridge and low component count.	Minidip
LS 346	Polarity guard with very low voltage drop	Integrated polarity guard, designed for MF dialling telephones. Drop is typically 100 mV with 10 mA line current.	Minidip
LS 5018 LS 5060 LS 5120	Overvoltage protection circuits	Integrated transient overvoltage suppressors for crowbar applications where very large transients (lightning, induced etc) can damage sensitive components. Breakover voltage (18V, 60V or 120V) is independent of transient rise time. Other features include very high current capability and failsafe operation.	Minidip
LS 496	Quad relay driver	Contains four drivers for bipolar relays. Each driver controlled by logic inputs all four drivers controlled by common disable input. All outputs short circuit protected.	16-pin DIP

Audio Amplifiers

AUDIO AMPLIFIERS FOR CAR RADIO

TYPE	FUNCTION	FEATURES	PACKAGE
TDA 2002	8W car radio amplifier	– Very few components. – High output current (3.5A). – Low distortion. – 8V - 18V supply. – Short circuit protection. – Thermal protection. – 40V load dump protection.	Pentawatt
TDA 2003	10W car radio amplifier		
TDA 2004	10+10W stereo amplifier for car radio	– High current capability (3.5A). – Loads down to 1.6Ω. – Low distortion/noise. – Output AC short circuit to ground. – 40V load dump protection.	Multiwatt-11®
TDA 2005	20W bridge amplifier for car radio	– High current capability (3.5A) – Low distortion/noise. – Output DC/AC short circuit to ground. – 40V load dump protection. – Protects loudspeaker in short circuits.	Multiwatt-11®

AUDIO AMPLIFIERS FOR TV/RADIO

TDA 1904	4W audio amplifier	– Output 3.5W into 4 Ω at 12V. – Supply 4V - 20V.	Powerdip 8 + 8
TDA 1905	6W audio amplifier with muting	– Output 5.5W into 4 Ω at 14V. – Supply 4V - 30V.	Findip
TDA 1908	8W audio amplifier	– Output 8W into 8 Ω at 22V. – Supply 8V to 30V.	Findip
TDA 1910	10W audio amplifier with muting	– Output 10W into 8 Ω at 24V. – Supply 8V - 30V. Designed for high quality TV sets.	Multiwatt-11®
TDA 2006	10W audio amplifier	– Output 12W into 4 Ω at 24V. – Supply 12V to 30V.	Pentawatt®
TDA 2008	12W audio amplifier	– Output 12W into 4 Ω at 24V. – Supply 10V to 28V.	Pentawatt®
TDA 2009	10+10W stereo amplifier	– Output 10 + 10W stereo into 4 Ω. – Low distortion (0.5%) and 8V - 28V supply range.	Multiwatt-11®
TDA 2822M	1 + 1W stereo amplifier	– For portable radios and cassette players. Delivers 1 + 1W stereo or 2W bridge. Supply range 1.8V-15V, low distortion and low quiescent current (6 mA).	Minidip

HiFi POWER AMPLIFIERS

TYPE	FUNCTION	FEATURES	PACKAGE
TDA 2030	HiFi Power amplifier	– Output 14W into 4 Ω at ± 14V. – Distortion 0.5% at 15 kHz and maximum supply ± 18V.	Pentawatt®
TDA 2030A	HiFi Power amplifier	– Output 18W into 4 Ω at ± 16V. – Distortion 0.5% at 15 kHz. – Maximum supply ± 22V. – Delivers 32W with two devices in bridge configuration.	Pentawatt®
TDA 2040	HiFi Power amplifier	– Output 22W into 4 Ω at ± 16V. – Distortion 0.5% at 1 kHz. – Maximum supply ± 20V.	Pentawatt®

Radio & TV Circuits

RADIO CIRCUITS

TYPE	FUNCTION	FEATURES	PACKAGE
TCA 3089	FM-IF Radio system	– High limiting sensitivity.. – High AMR. – High recovered audio. – Low distortion.	16-pin DIP
TCA 3189	FM-IF high quality radio system	– Very low distortion. – Improved S/N. – Programmable audio level.	16-pin DIP
TDA 1220L TDA 1220B	Low voltage AM/FM radio	– Designed for use in 3V-4.5V-6V portable radio. – High sensitivity. – Very low "tweet". – High signal handling. – Low battery drain.	16-pin DIP
TDA 2220	High quality AM/FM receiver	– Intended for car radio and portable/ home radio. – Ratio or quadrature detector. – AM/FM field meter.	20-pin DIP
TEA 1330	Stereo decoder	– Requires no inductors. – Wide supply range: 3V to 14V. – Excellent channel separation. – Low distortion.	16-pin DIP

TV SOUND CHANNELS

TDA 1190Z	Complete TV sound channel	– High limiting sensitivity (40 μV). – High AM rejection. – Low distortion. – High output power (4.2W into 16 Ω at 24V). – DC volume control.	Findip
TDA 3190	Complete TV sound channel		Powerdip 12 + 2 + 2
TDA 4190 TDA 8190	Complete TV sound channel	– DC volume and tone control. – Muting function. – Output power 4W into 16 Ω at 24V. – VCR in/out function.	Powerdip 16 + 2 + 2

TV DEFLECTION CIRCUITS

TYPE	FUNCTION	FEATURES	PACKAGE
TDA 1180P	Horizontal processor	– Includes complete horizontal processor function and protection circuits.	16-pin DIP
TDA 1170S	Vertical deflection system	Incorporates: – Synch. circuit – Oscillator and ramp generator – Power amplifier. – Flyback generator. – Voltage regulator.	Findip
TDA 1670A	Vertical deflection circuit	– Direct drive of 110° colour yoke (3.5A out, f = 50 Hz). – CRT screen protection. – Flyback generator. – Precision blanking pulse generator.	Multiwatt-15
TDA 1770A	Vertical deflection circuit	– 2.2A out, f = 50 Hz. – Flyback generator. – Precision blanking pulse generator. – CRT screen protection.	Powerdip 16 + 2 + 2
TDA 2170	TV vertical output circuit	– High efficiency power booster. – Reference voltage. – Flyback generator.	Multiwatt-15
TDA 2270	TV vertical output circuit		Powerdip 16 + 2 + 2
TDA 8170	TV vertical output circuit		Heptawatt
TDA 8180	Deflection processor	– No frequency or phase adjustments. – Countdown timing logic. – Automatic 50 Hz/60 Hz.	24-pin DIP

Radio & TV Circuits

TV VIDEO CIRCUITS

TYPE	FUNCTION	FEATURES	PACKAGE
TDA 440S	TV vision IF system	– Gain controlled vision IF amplifier. – Synchronous detector. – Positive and negative outputs.	16-pin DIP
TDA 4420	TV vision IF system with AFC	– High gain – high stability.. – Low intermodulation. – Fast AGC gating. – Large AFC out swing.	18-pin DIP

OTHER TV CIRCUITS

TYPE	FUNCTION	FEATURES	PACKAGE
TDA 4431/33	TV signal identification circuit and AFC interface	– Identification of TV stations. – Digital control signal for automatic search and AFC. – Ideal for electronic program memory tuning systems.	14-pin DIP
TDA 4092	5 bit binary to 7 segment Decoder Driver	– ROM mask option. – Standard configuration 2 digit (displays 1 to 32). – 5V supply.	24-pin DIP
TDA 2320	Infrared Receiver for Remote Control	– V_S = 5V. – Suitable for flash and carrier transmissions.	Minidip
TDA 4950	East-West correction	– Field correction in East-West direction. – Simple alignment. – Low dissipation.	Minidip

Tape Recorder / Player Circuits

PREAMPLIFIERS

TYPE	FUNCTION	FEATURES	PACKAGE
TDA 1054M TDA 2054M	Preamplifiers with ALC for cassette recorders	– V_S = 4V to 20V. – Large ALC range. – Good SVR. – Low distortion.	16-pin DIP
TDA 3410	Dual low noise tape preamplifier with autoreverse	– Very low noise. – High gain. – Low distortion. – Single supply operation (8V to 30V).	16-pin DIP
TDA 3420	Dual very low noise preamplifier		
TDA 2320A	Minidip stereo preamplifier	– Intended for portable cassette players and music centers. – Single/split supply. – Wide supply range (3V to 36V). – Very low consumption (0.8 mA). – Very low distortion. – Low noise.	Minidip

MOTOR SPEED REGULATORS

TYPE	FUNCTION	FEATURES	PACKAGE
TCA 900 TCA 910 TDA 1151	Motor speed regulators	– Intended for use as speed regulator for small DC motors. – Excellent stability vs. temperature. – $V_{S\ max}$ = 20V. – P_{tot} = 5W.	TO-126
TDA 3450	High performance motor speed regulator	– Bridge output for current up to 1A. – Particularly suitable for autoreverse car cassette players. – Digitally selected functions (inputs microprocessor compatible). – 5V to 18V supply. – Speed control without sensor.	Powerdip 16 + 2+ 2
TDA 7270S	Multifunction system for tape players	– Motor speed regulator. – Automatic stop. – Manual stop. – Pause cassette ejection. – Radio/player automatic switching. – Supply voltage: 6V to 18V.	Powerdip 8 + 8

Custom Circuits

FULL CUSTOM

SGS designs and produces custom bipolar ICs for a large number of leading manufacturers. Specialising in advanced technologies and packages for demanding applications, SGS is particularly strong in the industrial, automotive and telecommunications sectors.

A wide range of technologies is available for custom circuits, including low voltage, low noise, high voltage, high current and mixed analog/digital processes. SGS also offers packages of almost every type, ranging from the 8-pin small outline micropackage to the 15-lead Multiwatt plastic power package.

If you are interested in discussing custom chip designs contact your nearest sales office for more information.

ZODIAC CELL LIBRARY

Zodiac is a library cell system which allows customers with no specific knowledge of IC technology to design their own mixed analog/digital signal processing circuits. The library consists of 17 analog blocks, 16 I^2L logic blocks and an ECL prescaler. Individual transistors, diodes, capacitors and resistors can also be integrated.

The customer designs and evaluates the proposed design with the help of a series of development parts, each containing one or more of the library cells. When the breadboard functions correctly SGS takes the final drawings and lays out the appropriate cells in the smallest possible silicon area.

Zodiac is almost as fast as pre-diffused arrays but uses the silicon area more effectively. Zodiac chips are therefore cheap to develop and cheap to produce.